CLASSICAL TO QUANTUM TRANSPORT IN MULTI-DIMENSIONAL FIELD EFFECT TRANSISTORS

EDITED BY

NAVEEN KUMAR, PRATEEK KUMAR,
ANKIT DIXIT, AND PRABHAT SINGH

CRC Press
Taylor & Francis Group

Classical to Quantum Transport in Multi-Dimensional Field Effect Transistors

Classical to Quantum Transport in Multi-Dimensional Field Effect Transistors offers a wide range of topics with attractive images and informative explanations. It begins with an exploration of the fundamentals of field effect transistor (FET) functioning, emphasizing how behavior is governed by classical models. As the semiconductor industry pushes the boundaries of miniaturization and performance, Multi-Dimensional Field Effect Transistors (MuDFETs) and emerging material platforms are redefining the foundations of modern electronics. This book offers a deep and insightful journey through the evolving landscape of advanced FET architectures—from classical conduction models to quantum and ballistic transport regimes. Authored by experts across academia and research institutions, this book offers in-depth discussions on:

- Multi-Dimensional and Junctionless FETs: Design innovations enabling superior control, scaling, and performance.
- 2D Materials and Transition Metal Dichalcogenides (TMDCs): Harnessing atomically thin semiconductors for next-generation device engineering.
- Nanosheet Transistors: Unlocking new dimensions in charge transport and quantum confinement.
- Charge transport mechanisms from classical, semiclassical to ballistic regimes in nanosheet and nanowire FETs.
- Tunnel Field Effect Transistor (TFET)-Based Biosensors: Cutting-edge developments in label-free, ultra-sensitive detection for healthcare and environmental monitoring.
- Integration of FET platforms in nonlinear and quantum photonics using silicon nitride waveguides.

Whether you are exploring the quantum limits of device physics or developing real-world sensing solutions, this collection bridges theory and application in one compelling volume. With contributions from leading researchers and technologists, this book serves as a vital reference for academics, graduate students, and professionals working in nanoelectronics, semiconductor devices, biosensors, and photonic field.

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CRC Press
Taylor & Francis Group
Boca Raton London New York

CRC Press is an imprint of the
Taylor & Francis Group, an **informa** business

Designed cover image: Getty Images

First edition published 2026
by CRC Press
2385 NW Executive Center Drive, Suite 320, Boca Raton FL 33431

and by CRC Press
4 Park Square, Milton Park, Abingdon, Oxon, OX14 4RN

CRC Press is an imprint of Taylor & Francis Group, LLC

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ISBN: 978-1-032-89579-6 (hbk)
ISBN: 978-1-032-89655-7 (pbk)
ISBN: 978-1-003-54392-3 (ebk)

DOI: 10.1201/9781003543923

Typeset in Times
by codeMantra

Dedications

This book is dedicated to my beloved wife, Nisha Chaudhary, and our wonderful son, Zishaan Kumar, whose love and encouragement have been my greatest motivation. Special thanks to my parents, Smt. Indu Devi, and Shri. Rajpal Singh, for their unwavering support and sacrifices, and to my brother, Nitish Kumar, for always being there for me. I am deeply grateful to my mentors, Dr. Ashish Raman, and Prof. Vihar Georgiev, for their invaluable guidance and wisdom. I also extend my heartfelt appreciation to my supervisors, colleagues, and friends, whose support and encouragement have been instrumental in the completion of this work.

—Dr. Naveen Kumar

I dedicate this book to my beloved parents, my wife, Himani, and my daughter, Kiyana Vats. I am deeply grateful for everything you have done and continue to do for me. I would like to thank Prof. Maneesha Gupta, Dr. Kunwar Singh, and Dr. Ashish Raman for their unconditional guidance. This book is a testament to your belief in me and a symbol of my heartfelt appreciation.

—Dr. Prateek Kumar

I would like to dedicate this work to my parents, Mrs. Asha Dixit and Mr. Aditya Prakash Dixit, whose unconditional love and unwavering support have been the foundation of my academic journey. Their sacrifices and resilience continue to inspire me to strive for excellence. A heartfelt thank you to my wife, Mrs. Shashi Dixit, and my beloved daughter, Ms. Aadya Dixit, *for their constant encouragement and motivation, which have played a vital role in pushing me to do my best. I am also deeply grateful to my younger brother, Mr. Ankur Dixit, and all my family members and friends for their continued support and for standing by me through challenging times. Lastly, I extend my sincere gratitude to my mentor, Prof. Vihar Georgiev, at the University of Glasgow. His steadfast guidance and encouragement to explore new dimensions of research have made this work possible.*

—Dr. Ankit Dixit

I dedicate this book to my loving mother Shakuntala Singh, father Dinesh Singh, wife Sadhana Singh and brother Prasoon Singh, as a token of my appreciation for everything you have done and continue to do for me. Your love and support are the foundation of my success, and I am blessed to have you a part of my life. Your love and belief in me mean everything. This book is dedicated to you, as a symbol of my gratitude for all you've done.

—Dr. Prabhat Singh

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Preface

The evolution of semiconductor technology has been fundamental to the development of modern electronics, driving rapid advancements across a wide array of fields. While Complementary Metal Oxide Semiconductor (CMOS) technology has long stood at the forefront of semiconductor fabrication, the growing demand for low-power, high-performance, and multifunctional systems has ushered in a new era—one that calls for exploring alternative materials and innovative device architectures beyond conventional CMOS.

This book offers a comprehensive and in-depth exploration of emerging semiconductor technologies, addressing both the challenges and opportunities that accompany this transition. It highlights cutting-edge research in novel materials, advanced device structures, and circuit-level innovations, with a focus on their applications in next-generation electronics.

Key topics include the properties and potential of advanced semiconductor materials such as graphene, transition metal dichalcogenides (TMDs), and 2D materials. These materials promise significant improvements in device efficiency, thermal stability, and scalability, marking them as critical enablers of future technological breakthroughs.

This book also delves into state-of-the-art device architectures, including multi-dimensional field effect transistors (MuDFETs), nanosheet FETs, and gate-all-around (GAA) FETs. Applications in diverse domains such as biosensing, gas detection, and quantum transport are discussed in detail, along with crucial considerations like contact resistance, power optimization, and the shift from classical to quantum physics are also discussed.

A special emphasis is placed on niche and emerging applications, including high-performance silicon nitride waveguides for nonlinear and quantum photonics. The chapters provide valuable perspectives on the latest fabrication techniques, simulation tools, and industry trends, making this volume an essential resource for researchers, engineers, and students alike.

By blending theoretical foundations with practical insights and current research, this book aims to be a definitive guide to the evolving world of semiconductor technology. It is intended to inspire innovation, support ongoing research efforts, and empower readers to shape the future of electronics.

Short Explanation of Chapters Details

Effective collaboration among researchers in diverse domains—such as device fabrication, physical modeling, circuit design, advanced material-based sensing, and quantum mechanics—is essential for fostering innovation. By bridging these interdisciplinary fields, research can more efficiently transition from theoretical concepts to practical applications, accelerating the path from discovery to deployment. Chapters in this book cover the following.

Chapter 1: This chapter presents an overview of the advancement and evolution of MuDFETs. Various types of MuDFETs are discussed like FinFets, gate-all-around FETs, etc. along with their outstanding advantages. Ongoing research is centered on improving the synthesis and integration of 2D materials, developing new architectures for MuDFETs, and understanding the fundamental physics that govern their operation.

Chapter 2: This chapter examines the noticeable physical phenomena in transport mechanism of MuDFETs. The smaller-grade FETs become, the more cabalistic these effects are. This is frequently indicated in superior electron conduct and accelerated switching speeds caused by their better quantum confinement features and turned down scattering probabilities. This chapter looks at and analyzes limited structural alterations that have been implemented to ease such challenges and offers a proper justification for each of them.

Chapter 3: This chapter reviews different types of two-dimensional (2D) nanomaterials-based FETs, and compared to conventional silicon-based FETs. In this chapter, the structural representation and fabrication processes of two-dimensional material FETs and their electrical efficiency are examined in detail.

Chapter 4: This chapter provides an in-depth examination of transition metal dichalcogenides (TMDCs) as promising candidates for next-generation semiconductor technologies. TMDCs, represented by materials like MoS_2, WS_2, and WSe_2, exhibit remarkable electrical, optical, and mechanical properties due to their two-dimensional layered structure, making them highly attractive for nanoscale device applications. This chapter also offers insight into the transformative potential of TMDCs in enhancing device performance that could further unlock their potential in nanoelectronics and beyond.

Chapter 5: This chapter presents the complexities of nanosheet transistors, with a focus on the way ballistic transport models can be used to better understand and optimize their performance. It focuses on applying ballistic transport models to analyze the charge transport mechanisms in nanosheet transistors. This chapter aims to provide the information and resources needed to fully utilize nanosheet transistors in cutting-edge electrical applications by bridging the gap between classical and quantum transport models.

Chapter 6: This chapter presents a detailed examination of charge transport mechanisms in semiconductor devices, focusing on the transition from classical to semiclassical models that underpin modern field effect transistor (FET) architectures. By bridging classical and quantum frameworks, this chapter aims to provide insights into the intricate phenomena governing charge transport.

Chapter 7: This chapter presents a detailed analysis and simulations of junctionless multi-gate FETs' scaling capabilities. By leveraging 2D numerical simulations, this chapter aims is to gain valuable insights into the scaling capabilities and performance benefits of JL-DG and GAA MOSFETs, the way for next-generation low-cost nanoscale semiconductor devices.

Chapter 8: This chapter focuses on to provide the perfect criterion and investigate prospective directions of charge transport for enhancement depending on nanosheet transistors. It presents a summary of contemporary and forthcoming apparatus architectures that enable the continuation of device scaling. To understand the challenges involved in designing these devices, a brief analysis of the highly developed and future-generation semiconductor logic circuits will pave the path.

Chapter 9: This chapter explores the charge transport mechanism in nanosheet transistors. It covers the fundamental principles of nanosheet transistor operation, highlighting the unique quantum mechanical effects and material properties that contribute to their superior functionality. It also addresses recent advancements in fabrication techniques, such as chemical vapor deposition and molecular beam epitaxy, facilitating precise manipulation of nanosheet features. The discussion extends to the diverse applications of nanosheet transistors, from computing and data storage to sensor technologies and flexible electronics, showcasing their versatility and potential in next-generation devices.

Chapter 10: This chapter introduces a novel sensor device named as dual-metal double-gate metal strip-loaded extended source-Tunnel Field Effect Transistor (MS-ES-TFET) for breast cancer detection. The proposed biosensor is designed to optimize the electrostatic field and tunneling effects, which significantly improves the sensitivity for detecting breast cancer biomarkers.

Chapter 11: This chapter presents an extended source double-gate (ESDG) dielectric modulated (DM) TFET label-free biosensor using TCAD simulator. The nanogap cavity is considered near the source and drain regions of fixed HfO_2 layer to put up a large number of biomolecules. At last, the sensitivity of ESDG-DMTFET is compared with the sensitivity of existing FET/TFET-based biosensors.

Chapter 12: This chapter highlights the potential of FET gas sensors in diverse applications, from health and environmental monitoring to industrial safety, paving the way for future innovations in gas sensing technology.

Chapter 13: This chapter provides a thorough simulation and analysis of mode profiles in silicon nitride (SiN) waveguides. The results indicate that SiN waveguides are suitable for both linear and nonlinear applications in photonics due to their minimal propagation losses and strong optical confinement.

1 Introduction to Multi-Dimensional Field Effect Transistors (MuDFETs)

Mamataj Khatuna and Ekramul Kabir

1.1 INTRODUCTION

In the dynamic field of semiconductor technology, the pursuit of better performance, lower power usage, and smaller device sizes continues to drive breakthroughs. The transistor, a core component of modern electronics, has seen significant changes over time, fueling progress in computational capability and functionality. As conventional transistor designs near their physical scaling boundaries, there is a growing need for new architectures that can maintain the momentum of Moore's Law and meet the requirements of future electronic devices. Since Moore's Law was introduced in 1965, the number of transistors on a chip has doubled every 2 years [1]. Increased speed, reduced energy consumption, and lower costs are the main drivers of further circuit shrinking, offering enormous convenience and a diverse range of applications [2]. The ongoing shrinkage of silicon microelectronics has driven the exponential growth of integrated circuits for more than 50 years. Today, integrated circuits are ubiquitous, from desktops to smartphones. As the economy grows and digital technology advances, consumers demand higher portability and performance from these electronic devices. According to recent authoritative data and forecasts, the earnings from consumer electronics products are projected to reach US$365.54 billion in 2020, with the market expanding to US$450.39 billion by 2024 [3]. These devices are becoming increasingly miniaturized due to the use of very large-scale integration (VLSI). Metal oxide semiconductor field effect transistors (MOSFETs) serve as the fundamental components of VLSI [4]. As field effect transistor (FET) technology continues to scale down, extremely large-scale integration (ELSI) becomes achievable.

As traditional planar MOSFETs near their physical and performance constraints, engineers and researchers encounter mounting difficulties. These difficulties include short-channel effects (SCEs), leakage currents, and reduced gate control over the channel. The miniaturization of MOSFETs below 10 nm has proven to be particularly challenging, as conventional designs struggle to maintain a balance between performance and energy efficiency. The need for more powerful yet energy-efficient devices has driven the creation of new transistor architectures,

DOI: 10.1201/9781003543923-1

such as multi-dimensional field effect transistors (MuDFETs), which aim to overcome these scaling barriers by incorporating three-dimensional (3D) structures that enhance control and efficiency. MuDFETs represent an advanced type of transistor architecture developed to enhance gate control and minimize SCEs by extending the gate into multiple dimensions. The key idea is to expand the gate's control over the channel in a 3D space, offering greater influence over electron flow compared to traditional planar transistor designs [5]. This multi-directional control, enabled by advanced geometries, offers substantial advantages in terms of performance, energy efficiency, and scaling possibilities. A widely recognized example of MuDFETs is the FinFET (fin field effect transistor), a 3D structure in which the gate surrounds the channel (the fin) on several sides, enhancing control over electron flow through the channel [6].

As conventional transistors are reduced to smaller dimensions, the physical constraints of planar MOSFETs become increasingly evident. The main challenge arises from the gate's reduced capability to efficiently control the channel as the transistor size diminishes, resulting in SCEs like drain-induced barrier lowering (DIBL), higher power usage, and subthreshold leakage. In a planar MOSFET, the gate manages the channel from only one side—over the top of the channel. As the channel length shortens, the electric fields from the drain and source start to disrupt the gate's control over the channel, causing unwanted current leakage even when the transistor is in the inactive state. This leakage current escalates power consumption, especially in minimal-power consumption platforms like wearable electronics and smart home devices, where energy efficiency is crucial [7].

The shift from planar to 3D transistor designs has brought several significant advantages, extending the viability of Moore's Law. A major benefit of MuDFETs lies in their capability to mitigate SCEs, facilitating the ongoing reduction in transistor sizes while preserving both performance and energy efficiency. By surrounding the channel with the gate from multiple angles, MuDFETs offer enhanced electrostatic control, which decreases leakage currents and improves the on-state drive current (Ion). This contributes to quicker switching and reduced power usage, particularly in low-power applications like smartphones, tablets, and Internet of Things (IoT) devices [8–10]. Furthermore, MuDFETs enable higher drive currents because of their increased interaction between the gate and channel, supporting faster switching and superior performance in high-performance computing (HPC) and data center uses. The better electrostatic control also leads to a more favorable subthreshold swing (the rate at which the transistor transitions between on and off states), allowing for lower operating voltages and decreased power consumption. This is crucial for battery-operated devices, where power efficiency is key to prolonging battery life. Additionally, as the industry continues to push toward smaller nodes, new materials such as 2D materials (e.g., transition metal dichalcogenides (TMDs) and graphene) may need to be integrated with MuDFET structures to boost performance and tackle challenges like heat dissipation and quantum effects [11–13].

As semiconductor technology nears the physical constraints of conventional planar transistors, MuDFETs have emerged as a vital solution. With this in consideration, this chapter aims to provide a thorough overview of the design framework for MuDFETs and comprehensively examine the different variations of MuDFETs.

This framework is based on fundamental research papers from academic sources. Following this, we explore the application of these design principles in the fabrication of various FETs, such as tri-gate FETs, FinFETs, nanowire FETs, gate-all-around (GAA) FETs, and carbon nanotube FETs, derived from additional resources, along with their numerous uses.

1.2 WHAT ARE MUDFETS?

MuDFETs constitute a breakthrough in semiconductor technology, especially in addressing the constraints of conventional planar MOSFETs. As the demand for faster, smaller, and more power-efficient transistors increases, MuDFETs have emerged as an effective alternative by extending transistor structures into three dimensions, thereby improving performance and scaling potential. MuDFETs, including well-known types such as FinFETs [14,15], GAAFETs [16–18], and nanosheet/nanowire FETs [19], are regarded as critical to advancing Moore's Law in the post-5 nm era.

MuDFETs diverge from traditional two-dimensional planar MOSFETs by incorporating a 3D design. In a standard MOSFET, the gate controls the channel from a single direction (above the channel), which results in significant leakage currents and SCEs as device dimensions decrease. MuDFETs, by contrast, envelop the channel from multiple directions, providing superior electrostatic manipulation of the charge carriers within the channel. This leads to reduced leakage currents and enhanced gate control, even at nanometer-scale dimensions. MuDFETs are predominantly fabricated using silicon, but as device scaling progresses beyond the 5 nm node, alternative materials like silicon-germanium (SiGe), III–V semiconductors (such as InGaAs), and even 2D materials like TMDs and graphene are being explored for their superior electrical properties. The manufacturing of MuDFETs necessitates cutting-edge lithography methods, such as extreme ultraviolet (EUV) lithography, to create the small, intricate structures essential for multi-gate configurations [20,21]. While MuDFETs operate similarly to conventional MOSFETs, they feature significant structural adaptations. Their functionality is based on regulating current flow through a semiconductor channel by inducing an electric field through the gate. The main distinction in MuDFETs is that the gate surrounds the channel on multiple sides (either three sides in FinFETs or entirely in GAAFETs), enhancing the electric field's influence over the channel and providing better control over the movement of charge carriers. In a typical FinFET, when electric potential is applied to the control terminal, the electric field can more effectively deplete the channel region since the gate exerts control from three sides. This improves the subthreshold slope, meaning the device can switch more efficiently between on and off states. In GAAFETs, this effect is even stronger, as the gate fully encloses the channel, offering the optimal control over current flow and further minimizing leakage [22,23].

Unlike conventional planar MOSFETs, where the gate controls the channel from a single direction (above), MuDFETs enable the gate to engage with the channel from multiple directions. This multi-dimensional setup gives rise to various types of MuDFETs, which are discussed in detail.

1.3 TYPES OF MuDFETs

MuDFETs represent a category of sophisticated FET that features multiple gates to improve the regulation of current in the transistor channel, resulting in superior performance at reduced dimensions. Various kinds of MuDFETs have been created, each providing unique benefits for uses. The primary types consist of the following.

1.3.1 FinFETs (Fin Field Effect Transistors)

As the semiconductor sector delved into the nanoscale realm, the constraints of traditional transistor designs became apparent. To address these issues, FinFET technology emerged as a revolutionary advancement in the early 21st century. FinFETs introduced an innovative 3D transistor configuration, with the transistor channel encircling fin-like structures [24]. This configuration offered superior electrostatic control, alleviating problems related to power leakage and enhancing overall performance. The integration of FinFETs has been crucial in maintaining the momentum of Moore's Law, facilitating the ongoing reduction in transistor size and progression in semiconductor technology. Nevertheless, as the industry moves toward even smaller transistor sizes, exploring alternatives to FinFETs becomes increasingly essential [25]. The drive for progress beyond FinFETs is fueled by the rising difficulties concerning power consumption, heat management, and manufacturability at nanoscale dimensions. Researchers and engineers are vigorously investigating alternative transistor designs to tackle these issues and set the stage for the next phase of semiconductor advancement [26]. This exploration includes innovative designs such as nanosheet transistors and tunnel field effect transistors (tunnel FETs), each providing unique benefits in performance and energy efficiency. Due to SCEs, device performance deteriorates, rendering devices incompatible below 20 nm [27]. To improve gate control over the channel, the semiconductor industry has transitioned to a different FET, namely the FinFET. Essentially, a MOSFET built on a bulk or silicon-on-insulator (SOI) substrate, it features a gate fabricated around two, three, or all sides of the channel to create a multi-gate structure. FETs are referred to as "FinFET" because their source and drain regions form fins on the Si surface. They are also known as multi-gate FETs (MGFET) [28]. Figure 1.1 shows the basic structure of a FinFET.

There are several benefits of FinFET compared to bulk MOSFET, including a superior voltage gain. FinFETs offer a voltage gain that is two to three times greater than that of MOSFETs. Additionally, these FETs exhibit significantly improved electrical coupling between the front and back transistors. Their dual-layer design also allows for advanced circuit specifications [29]. Since conventional MOSFETs lack effective gate control over the channel and are unable to handle noise injection at technology nodes below 32 nm, this enhanced technology has been developed.

Classifications: FinFETs are essentially divided into two types: (i) Independent gate FinFET (IGF) and (ii) short gate FinFET (SGF).

SGF is generally favored over IGF due to its lower cost, reduced area usage, and superior on and off current characteristics. SGF are also categorized based on their

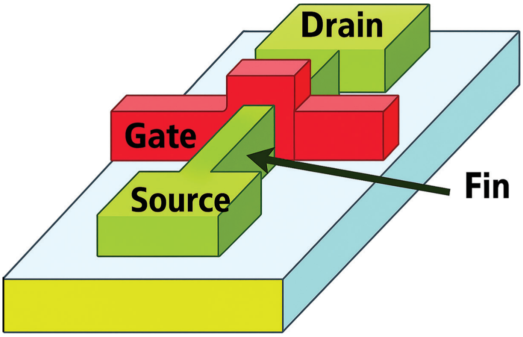

FIGURE 1.1 A basic structure of a FinFET.

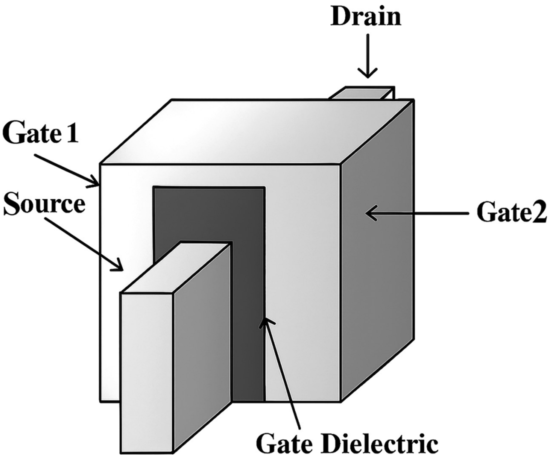

FIGURE 1.2 A basic structure of asymmetric gate work function FinFET (ASGF) [30].

asymmetric device parameters. This SGF is alternatively referred to as asymmetric short gate FinFET (ASGF). Figure 1.2 illustrates the structure of the ASG FinFET, which can be produced using two different dopants to create two variations of gate stacks (shorted gates with differing dopants) [30]. Table 1.1 illustrates the analysis between IGF and SGF (Figure 1.3).

1.3.2 TRI-GATE FETs

Tri-gate FETs signify a significant progress in semiconductor technology, especially in overcoming the constraints of planar transistors. As transistor proportions continue to decrease consistent with Moore's Law, conventional planar transistors encounter escalating difficulties related to leakage currents and reduced control over the channel. Tri-gate FETs provide a resolution by offering superior electrostatic control over the channel through a 3D configuration. This structure improves performance,

TABLE 1.1
Comparison between Independent Gate FinFET (IGF) and Short Gate FinFET (SGF)

Feature	Independent Gate FinFET	Short Gate FinFET
Gate structure	Two independent gates	Two gates are shorted together
Gate control	Independent control of each gate (can be biased separately)	Single control as both gates is electrically shorted
Operational flexibility	High flexibility due to separate gate biasing	Less flexible as gates are shorted and biased together
Power consumption	Can optimize power using gate biasing strategies	Higher power consumption due to single biasing control
Low-power applications	More appropriate for low-power applications	Less appropriate for low-power applications
Circuit design	More design options due to flexible gate control	Limited design flexibility
Applications	Used in advanced low-power designs, sensor circuits	Common in conventional digital circuits for speed
Leakage control	Improved leakage control by varying gate bias	Limited leakage control

Note: n-FinFETs and p-FinFETs: In Figure 1.3, we observe the n-FinFETs employing SGF and IGF, which have a work function of 4.4 eV [30].

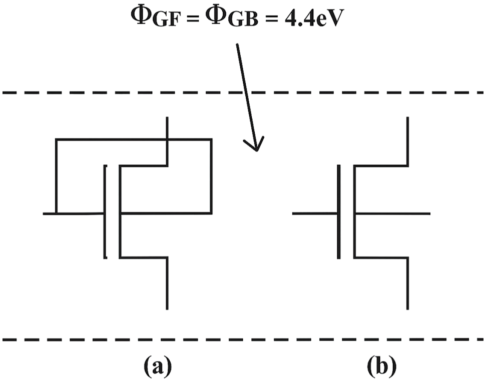

FIGURE 1.3 A schematic diagram of n-FinFET: (a) using short gate FinFET and (b) using independent gate FinFET [30].

energy efficiency, and scalability in contemporary microprocessors and memory components. FinFET configurations, particularly those using bulk-Si wafers as substrates, face notable challenges during fabrication due to the need for creating thin Si fins with consistent width and high aspect ratios (>1), as well as requiring a deep retrograde doping profile at the fin channel's base to mitigate sub-fin leakage between source and drain regions. Tri-gate presents a more progressive approach for continued miniaturization, demanding a lower aspect ratio of the channel and permitting a less steep retrograde doping gradient [31]. The Tri-gate MOSFET utilizes three gates, with a single gate stacked atop two vertical gates, forming a square or rectangular cross-section (as depicted in Figure 1.4a) and provides three times the area for electron movement. The width of the gate is the total of all three sides of the semiconductor body. This transistor is predominantly utilized in fully depleted transistor applications [32,33]. Intel asserts that tri-gate transistors reduce leakage and consume less power compared to current transistors [34]. They offer enhanced gate electrostatic control of the conducting channel and dynamic control of V_T, resulting in better performance. Back gate biasing is a potential method to adjust V_T by leveraging the body effect [35]. Figure 1.5 illustrates the variation of V_T relative to channel width. As the width increases in SOI FINFETs, the distance between the two gate electrodes also expands, thereby reducing gate control over the channel.

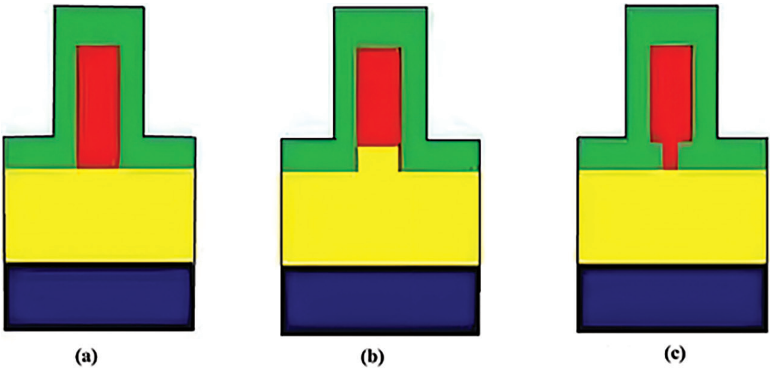

FIGURE 1.4 A basic structure of (a) tri-gate FET, (b) PI-gate, and (c) omega-gate FET [33].

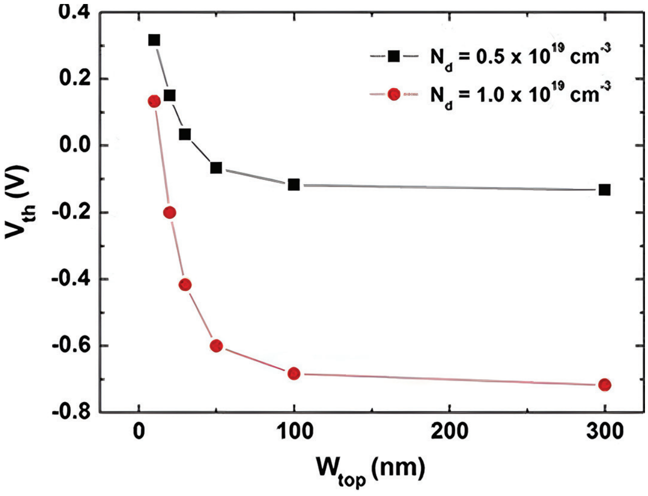

FIGURE 1.5 Variation of V_T sensitivity to channel width (W_{top}) [36].

However, in tri-gates, the presence of the top gate stack means that channel control does not significantly diminish, thus reducing the sensitivity of V_T relative to channel width [36].

The primary concern with such devices is the corner effect, which arises from the accumulation of trapped charges at the corners. This issue results in increased temperature, reliability problems, elevated leakage current, and exacerbates SCEs. The most effective way to mitigate leakage current and, consequently, the corner effect is to round off the corners [37]. The electrostatic performance of tri-gate is enhanced by extending the gate electrode's sidewalls into the buried oxide (illustrated in Figure 1.4b) to a certain depth and underneath the channel region (shown in Figure 1.4c), referred to as a "-gate" and "-gate," respectively [33]. The terms "Pi FinFET" and "Omega FinFET" are used because the gates in these devices encircle the semiconductor body like the Greek letters Pi and Omega [38]. These devices effectively have between three and four gates [33], as shown in Figure 1.4. In the Pi-gate configuration, the gate extension shields the channel's rear from electric field lines originating from the drain, which acts as the actual back gate [39], while the omega-gate features a "virtual" fourth gate beneath the semiconductor body due to the presence of a gate fringe field, addressing SCEs.

The advent of tri-gate FETs enabled further scaling consistent with Moore's Law by overcoming the constraints of planar transistors, which had hit their physical and performance limits at smaller scales [40,41]. A major milestone in tri-gate FET technology occurred in 2011 when Intel launched its 22 nm "Ivy Bridge" processors, marking the first significant use of 3D transistors in commercial products by a major chip manufacturer [42].

Applications of tri-gate FETs:

- **High-Performance Computing**: Tri-gate FETs are extensively used in modern CPUs and GPUs, where their ability to switch faster and consume less power is critical for performance.
- **Low-Power Devices**: Mobile devices and embedded systems benefit from tri-gate FETs, as they help extend battery life by reducing power consumption.
- **Memory Devices**: Tri-gate FETs are also finding applications in memory technologies, including static random access memory (SRAM) and dynamic random access memory (DRAM), where their low leakage current is particularly advantageous.

As we progress toward even smaller nodes (5 nm, 3 nm, and beyond), tri-gate FETs are anticipated to continue being a fundamental technology. Nonetheless, emerging transistor configurations such as nanosheet FETs and GAA FETs are under investigation as possible successors to tri-gate FETs, promising enhanced control over the channel and further minimizing leakage currents. Tri-gate FETs have transformed semiconductor technology, delivering better performance, lower power consumption, and superior scalability compared to conventional planar transistors [43,44]. Despite the obstacles in production and thermal management, they remain an essential technology for advancing contemporary computing and sustaining the momentum of Moore's Law.

1.3.3 GATE-ALL-AROUND (GAA) FETs

GAA FETs represent a next-generation transistor design developed to overcome the constraints of conventional planar and FinFET architectures. GAA FETs provide enhanced electrostatic regulation of the channel by encircling it with the gate, decreasing leakage currents, and allowing better scalability for advanced process nodes (sub-5 nm technologies).

GAA FETs are viewed as an advancement of FinFETs, which have been the prevailing design in semiconductor fabrication at the 22, 14, and 7 nm process nodes. FinFETs, which encase the gate around three sides of the channel, offered superior electrostatic control compared to traditional planar transistors. However, as the scaling trend approaches 5 nm and smaller, the shortcomings of the FinFET design become apparent. GAA FETs enhance this by permitting the gate to encompass the channel completely. The shift to GAA FETs is motivated by the need to manage SCEs, cut power consumption, and enhance performance in ultra-scaled technology nodes [45]. The hallmark of GAA FETs is their capability to encase the gate entirely around the channel, delivering near-ideal electrostatic control. This differs from FinFETs, where only three sides of the channel are gated. The GAA design employs a nanowire or nanosheet structure for the channel, surrounded by the gate on all sides. A basic structure of GAA FETs is shown in Figure 1.6 [46].

1.3.3.1 Advantages of GAA FETs

- **Enhanced Electrostatic Control**: GAA FETs' gate surrounds the channel, providing better electrostatic control and significantly reducing SCEs compared to FinFETs.
- **Superior Performance**: Due to improved gate control, GAA FETs offer better switching characteristics and drive currents, particularly in scaled-down nodes.

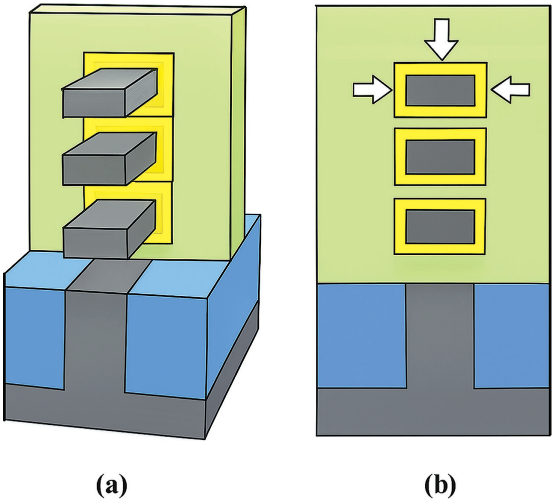

FIGURE 1.6 A schematic diagram of GAA [46].

- **Lower Leakage and Power Consumption**: The all-around gate reduces leakage currents, contributing to lower power consumption, a critical requirement for mobile and HPC applications [47].

As semiconductor nodes decrease in size, preserving gate control and minimizing leakage become essential. GAA FETs offer superior scalability compared to FinFETs, enabling greater packing density without compromising performance or increasing power usage. This positions GAA FETs as the optimal choice for sub-5 nm nodes and beyond. TSMC and Samsung have both announced their intentions to adopt GAA FETs at the 3 nm node, with GAA technology expected to advance Moore's Law into the future [48,49]. Despite the advantages of GAA FETs, their production is more intricate than that of FinFETs. The process entails the development of nanoscale channels (such as nanowires or nanosheets), necessitating sophisticated lithography and etching methods. The exact stacking of nanosheets or nanowires in a multi-layer arrangement further adds to the complexity of manufacturing [50,51]. Both Samsung and TSMC are vigorously advancing GAA technology for the 3 nm node and beyond. Samsung's GAA design is termed multi-bridge channel FET (MBCFET), featuring a nanosheet structure for improved performance and scalability. TSMC has stated that its version of GAA FETs will be prepared for mass production at 3 nm, drawing on their FinFET manufacturing expertise [52–54]. Intel has also expressed interest in transitioning to GAA FETs for future nodes [55,56]. Although GAA FETs mark a major advancement, their success hinges on addressing fabrication challenges, especially at scale. As semiconductor nodes keep shrinking, hybrid architectures that integrate GAA FETs with other advanced technologies, such as tunnel FETs (TFETs) or ferroelectric FETs (FeFETs), may arise. These hybrid solutions could push Moore's Law even further, facilitating the creation of transistors with exceptional performance and efficiency [57–60].

1.3.4 NANOWIRE FETs

Nanowire field effect transistors (NWFETs) have captured significant attention due to their potential to propel the next generation of nanoscale electronics. Featuring a unique one-dimensional structure, nanowires provide several benefits, including improved electrostatic control, scalability, and elevated surface-to-volume ratios. This enables NWFETs to address some of the constraints encountered by traditional planar transistors, positioning them as promising candidates for future applications in high-performance electronics, sensors, and even quantum computing. In this discussion, we will expand on the structural, operational, and technological facets of nanowire FETs [61–63]. NWFETs are distinguished by their cylindrical nanowire channels, which are generally composed of materials such as silicon, III–V semiconductors (e.g., InAs, GaAs), or carbon nanotubes (CNTs). These nanowires may be either synthesized through bottom-up methods (such as chemical vapor deposition) or produced using top-down techniques (such as etching processes) [64,65].

Nanowire FETs can have several gate configurations depending on the way the gate electrode is placed. These include:

- **Top-Gated**: A gate placed above the nanowire channel.
- **Gate-All-Around (GAA)**: A gate surrounding the entire nanowire, providing improved electrostatic control.
- **Dual-Gated**: Two gates controlling the channel from opposite sides.

Among these, the GAA configuration provides superior gate control, particularly in subthreshold regions, which is vital for scaling down devices to the nanometer scale. A schematic diagram illustrating the method used to fabricate n-FETs is shown in Figure 1.7 [66]. Nanowire FETs function on principles akin to those of traditional MOSFETs. They depend on an electric field created by the gate to adjust the conductivity of the nanowire channel. Nonetheless, the cylindrical shape

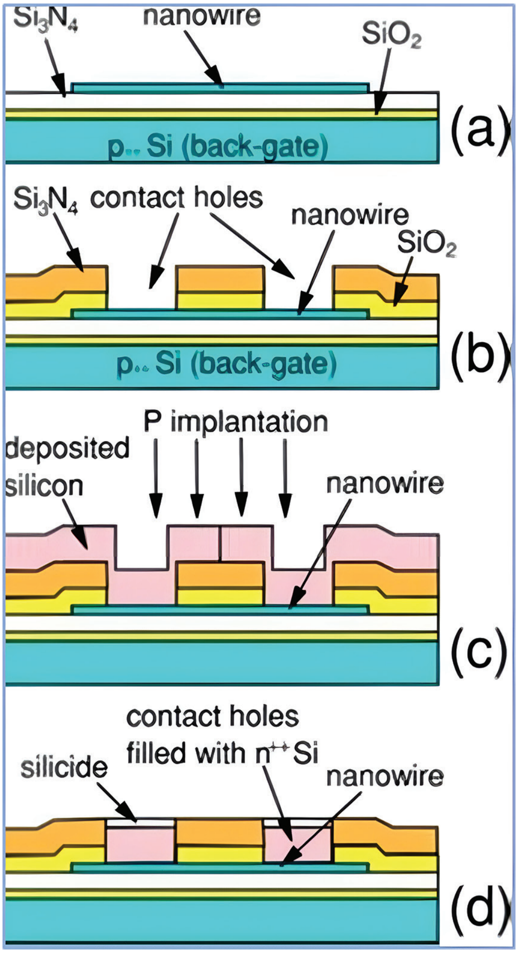
Si_3N_4
nanowire
SiO_2
p++ Si (back-gate)
(a)
Si_3N_4
contact holes
nanowire
SiO_2
p++ Si (back-gate)
(b)
P implantation
deposited silicon
nanowire
(c)
contact holes filled with n^{++} Si
silicide
nanowire
(d)

FIGURE 1.7 A schematic diagram illustrating the method used to fabricate N-FETs width [66].

of nanowires provides enhanced electrostatic regulation over the channel, mitigating SCEs that affect conventional FETs at nanoscale sizes. Elevated Surface-to-Volume Ratio: The narrow diameter of nanowires leads to a greater surface-to-volume ratio, which boosts carrier mobility and sensitivity to external fields, making it particularly advantageous for sensor applications [67–70].

1.3.4.1 Material Considerations

- **Silicon Nanowires**: Silicon remains the dominant material due to its compatibility with existing complementary metal oxide semiconductor (CMOS) technologies. However, silicon nanowires face limitations in carrier mobility, especially in p-type channels [71].
- **III–V Semiconductor Nanowires**: Materials like InAs and GaAs provide much higher electron mobilities compared to silicon, making them attractive for high-speed applications. InAs nanowires have shown potential for low-power applications due to their small bandgap [72].
- **Carbon Nanotubes and Graphene Nanoribbons**: These carbon-based nanostructures offer excellent electrical and mechanical properties, including ballistic transport and high carrier mobility. They have been explored for use in ultrahigh-performance NWFETs [73].

1.3.4.2 Advantages

NWFETs present several advantages over conventional transistors, particularly in terms of scalability and performance at nanoscale dimensions:

- **Improved Short-Channel Control**: The GAA structure provides enhanced electrostatic control over the channel, reducing SCEs that degrade performance in ultrasmall devices.
- **Reduced Power Consumption**: Due to their better control over the channel, NWFETs can operate at lower voltages, reducing power consumption, which is crucial for energy-efficient electronics.
- **High-Speed Operation**: III–V semiconductor nanowires, with their higher electron mobilities, allow NWFETs to operate at higher frequencies, making them suitable for radio-frequency (RF) and high-speed digital applications [74].

1.3.4.3 Challenges and Limitations

Despite their promising attributes, NWFETs face several challenges:

- **Fabrication Complexity**: The precise fabrication of nanowires with controlled dimensions and doping profiles remains a significant challenge, especially when considering large-scale production.
- **Contact Resistance**: High contact resistance between the nanowire and metal electrodes can degrade device performance. Engineering low-resistance contacts is an area of ongoing research [75].
- **Variability and Reliability**: As devices shrink to the nanoscale, variability in device characteristics (due to surface roughness, defects, etc.) becomes more pronounced, which can affect the reliability of NWFETs [76].

1.3.4.4 Applications

NWFETs Have Several Emerging Applications:

- Their scalability and superior performance at small dimensions make NWFETs ideal candidates for the next generation of transistors in microprocessors and memory devices. Because of their elevated surface-to-volume ratio, nanowires are extremely responsive to alterations in their surroundings, making NWFETs excellent candidates for biosensing, chemical sensing, and gas detection applications. Semiconductor nanowires have been explored for quantum computing, particularly in the context of Majorana fermions, which could be used for fault-tolerant quantum information processing.

The development of nanowire FETs is still in its early stages, and ongoing research focuses on overcoming the technical challenges associated with their fabrication and integration [77–79]. Some key research directions include:

- **Heterostructure Nanowires**: By combining different materials along the length of the nanowire, it is possible to engineer devices with novel properties, such as higher carrier mobilities or integrated optoelectronic functionality [80].
- **Flexible Electronics**: NWFETs are also being explored for use in flexible and wearable electronics, where their high performance and small size could enable new types of devices [81].

Nanowire FETs represent a significant advancement in the realm of nanoscale electronics. Their unique structure, material properties, and potential for enhanced performance make them key candidates for future technological applications. However, challenges related to fabrication, variability, and large-scale integration need to be addressed for them to become commercially viable. As research progresses, NWFETs could play a crucial role in advancing semiconductor technology beyond the limits of traditional scaling.

1.3.5 CARBON NANOTUBE FETS (CNTFETS)

Carbon Nanotube Field Effect Transistors (CNTFETs) are considered one of the most promising substitutes for conventional silicon-based transistors in microelectronics. The distinctive characteristics of CNTs, such as elevated carrier mobility, adjustable bandgap, and ballistic conduction, render CNTFETs a viable option for prolonging Moore's Law in semiconductor technology. As we near the boundaries of silicon technology regarding miniaturization, energy consumption, and performance, CNTFETs present the potential to surmount these constraints. CNTFETs utilize CNTs as the channel material rather than silicon. CNTs can be either single-walled (SWCNTs) or multi-walled (MWCNTs), depending on the quantity of rolled graphene layers. The tubular configuration of CNTs imparts distinctive electrical characteristics that are crucial for CNTFET functionality. CNTs can be either metallic or semiconducting depending on their chirality, which influences their appropriateness for transistor uses. Semiconducting CNTs are especially beneficial in FETs due to their ability to provide the switching behavior necessary for digital logic circuits. CNTFETs share a similar fundamental structure with conventional FETs, including source, drain, and gate terminals. However, the channel material in CNTFETs is a carbon nanotube, and its diameter and chirality affect the device's efficiency [82].

1.3.5.1 Features of CNT Structure

- **Chirality and Bandgap**: The electronic properties of a CNT are determined by its chirality, which defines whether it behaves as a metal or semiconductor. Semiconducting CNTs are used in FETs, and their bandgap can be tuned by controlling the diameter of the nanotube.
- **High Mobility**: Electrons and holes move through CNTs with minimal scattering due to the quasi-one-dimensional structure, resulting in high carrier mobility, which is crucial for high-speed transistor operation [83].
- **Ballistic Transport**: At nanoscale dimensions, charge carriers can move through CNTs without experiencing resistance due to collisions, allowing for ballistic transport over short distances. This minimizes power loss and enhances the performance of CNTFETs.

The operational principle of CNTFETs resembles that of silicon-based MOSFETs. In CNTFETs, a voltage is exerted to the gate electrode, which influences the carrier density in the CNT channel. When the gate voltage exceeds a certain threshold, current flows between the source and drain via the CNT channel. This current is managed by the gate voltage, enabling the CNTFET to act as a switch [84]. One of the significant benefits of CNTFETs compared to traditional MOSFETs is that CNTs provide higher carrier mobility and ballistic transport, which decreases switching delays and power consumption. Furthermore, CNTs can function at lower voltages, resulting in enhanced energy efficiency. A schematic diagram of CNFET and its top-view approach are shown in Figure 1.8 [82].

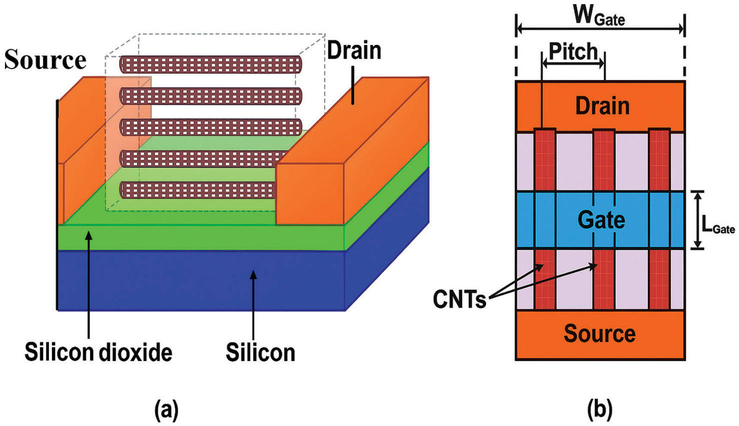

FIGURE 1.8 (a) A schematic diagram of carbon nanotube field effect transistor (CNFET) and (b) top-view approach [82].

1.3.5.2 Advantages of CNTFETs

- **High Electron Mobility**: CNTFETs offer electron mobility 10–100 times higher than silicon-based transistors, allowing faster switching and lower power consumption.
- **Low Power Consumption**: Due to their reduced size and improved material properties, CNTFETs require lower operating voltages and dissipate less power, making them suitable for low-power applications.
- **Scalability**: As CNTFETs have nanometer-scale dimensions, they are more scalable than traditional silicon transistors, which face limitations due to SCEs as dimensions shrink.
- **Improved Performance at Nanoscale**: Unlike silicon-based transistors that face performance degradation at smaller scales, CNTFETs maintain their high performance at nanoscale dimensions.
- **Ballistic Transport**: The one-dimensional nature of CNTs allows for ballistic transport of carriers over short distances, reducing scattering and enhancing speed and efficiency.

Despite their many advantages, CNTFETs face several challenges that need to be addressed before they can replace silicon-based transistors in large-scale manufacturing: Producing semiconducting CNTs with consistent chirality is a significant challenge, as metallic CNTs can compromise the performance of CNTFETs. Methods to separate metallic and semiconducting CNTs are still being refined. Proper alignment and placement of CNTs during fabrication are crucial to ensure consistent device performance. Current fabrication techniques are not yet mature enough to achieve this at a large scale. High contact resistance between CNTs and metal electrodes can limit the performance of CNTFETs. Research is ongoing to improve the interfaces between CNTs and metal contacts. Integrating CNTFETs with existing silicon-based CMOS technology presents challenges in terms of manufacturing compatibility and process optimization.

1.3.5.3 Types of CNTFETs

1.3.5.3.1 Schottky Barrier CNTFETs (SB-CNTFETs)

Schottky Barrier CNTFETs use Schottky barriers at the supply and sink contacts. These barriers can affect the device's I–V characteristics, and the transition behavior is largely determined by the modulation of the Schottky barriers. While SB-CNTFETs offer high-speed operation, they suffer from high contact resistance and are sensitive to variations in gate voltage [85].

1.3.5.3.2 MOSFET-Like CNTFETs

In MOSFET-like CNTFETs, metal electrodes form ohmic contacts with the CNT channel. This type of CNTFET has better control over the channel current and reduced contact resistance compared to SB-CNTFETs. MOSFET-like CNTFETs are more suitable for digital applications due to their better switching behavior.

1.3.5.4 Applications of CNTFETs

CNTFETs have the potential to revolutionize several fields of microelectronics, offering benefits in terms of power efficiency, scalability, and performance [86]. Some of the key applications include:

- **Low-Power Digital Circuits**: CNTFETs are promising candidates for low-power logic circuits, as they offer superior performance at low voltages compared to silicon-based transistors.
- **High-Frequency RF Circuits**: Due to their high electron mobility and ballistic transport properties, CNTFETs can operate at high frequencies, making them suitable for RF applications.
- **Flexible Electronics**: CNTFETs can be fabricated on flexible substrates, which makes them suitable for use in flexible electronic devices and sensors.
- **Memory Devices**: CNTFETs can be used in memory devices such as SRAM and DRAM, offering higher speed and lower power consumption compared to traditional silicon transistors.

Research on CNTFETs is continuing, with substantial advancements being made in overcoming the issues related to chirality regulation, manufacturing methods, and contact impedance. The possibility for CNTFETs to surpass silicon-based transistors at nanoscale sizes makes them a formidable candidate for upcoming generations of microelectronics. As production methods advance, CNTFETs could be incorporated into high-efficiency, low-energy electronic systems, pushing the frontiers of semiconductor technology. CNTFETs signify a notable progression in transistor technology, providing multiple benefits over conventional silicon-based transistors, particularly as the semiconductor sector progresses toward smaller and more energy-efficient devices. Nevertheless, obstacles such as chirality regulation, manufacturing methods, and contact impedance need to be addressed before CNTFETs can be widely commercialized. The continuous research in this domain is encouraging, and CNTFETs might play a pivotal role in the future of nanoelectronics.

1.4 APPLICATIONS OF MULTI-DIMENSIONAL FETs

Multi-dimensional FETs, such as FinFETs (3D), nanowire FETs, and 2D material-based FETs, represent a leap forward from conventional planar FETs. These structures enhance control over SCEs, reduce leakage currents, and offer improved power and speed characteristics, making them highly suited for a wide range of advanced applications.

1.4.1 High-Performance Computing (HPC)

Multi-dimensional FETs are a key technology in HPC, where miniaturization and improved efficiency are critical. Devices like FinFETs offer superior control over leakage currents and electrostatic properties, allowing for higher switching speeds and lower power consumption in processors [87].

1.4.2 INTERNET OF THINGS (IOT) DEVICES

IoT devices often require power-efficient, miniaturized transistors for sensing, processing, and communicating. FinFETs and nanowire FETs allow for integration into small-scale chips that combine functionality with low power consumption, ideal for energy-sensitive applications like smart sensors and wearable devices [88].

1.4.3 5G AND RF APPLICATIONS

In RF and 5G communication systems, FETs like FinFETs and nanowire FETs are crucial for improving transistor frequency response and minimizing parasitic effects. Their enhanced control over leakage currents at high frequencies makes them ideal for amplifiers and transceivers used in modern communication systems [89].

1.4.4 NEUROMORPHIC COMPUTING

Multi-dimensional FETs like FinFETs are essential in neuromorphic computing systems, which mimic biological neural networks. These transistors offer better scalability and power efficiency, allowing for more effective emulation of brain-like structures and functions [90].

1.4.5 QUANTUM COMPUTING

2D material-based FETs (e.g., using graphene or TMDs) are promising for quantum computing due to their excellent electrical properties at the nanoscale. These materials offer quantum confinement effects, making them suitable for qubits and quantum gates [91].

1.4.6 ARTIFICIAL INTELLIGENCE (AI) HARDWARE

FinFETs and 3D nanowire FETs are increasingly used in AI accelerators, where HPC is needed to process large datasets efficiently [92]. The reduced power leakage and improved switching speed of these FETs are ideal for AI tasks such as machine learning and deep learning.

1.4.7 BIOMEDICAL DEVICES

Multi-dimensional FETs have found applications in biosensors, where they can detect small signals such as electrical changes in cells. 2D material-based FETs (e.g., graphene) are used for developing sensitive sensors that can detect biomarkers, making them ideal for medical diagnostics [93].

1.4.8 FLEXIBLE AND WEARABLE ELECTRONICS

2D FETs made from materials like graphene and molybdenum disulfide (MoS_2) are increasingly used in flexible and wearable electronics [94]. These FETs can be integrated into flexible substrates, enabling a new generation of bendable and stretchable devices.

1.4.9 Power Electronics

In power electronics, multi-dimensional FETs, such as silicon carbide (SiC)-based or gallium nitride (GaN)-based devices, are employed to handle high-voltage and high-power applications. They provide improved efficiency and thermal performance for devices like inverters, power converters, and electric vehicles (EVs) [95].

1.4.10 Memory Technologies

Multi-dimensional FETs are increasingly being applied in memory technologies, particularly for dynamic RAM (DRAM) and non-volatile memory, where power efficiency and data retention are critical. The reduced SCEs in multi-dimensional FETs allow them to scale further without significant power penalties [96].

Multi-dimensional FETs are pivotal for advancing modern electronics. They provide key improvements in power efficiency, scaling, and performance, enhancing their versatility, from HPC to flexible electronics. The continuous development of these FETs will play a central role in the evolution of future semiconductor technologies.

1.5 CHALLENGES AND FUTURE DIRECTIONS

MuDFETs represent a critical advancement in semiconductor technology, addressing scaling challenges that limit traditional planar MOSFETs. However, their development and implementation come with several challenges and future directions that need to be explored. As MuDFETs are multi-gate devices with complex 3D structures, their fabrication involves intricate processes. This complexity increases manufacturing costs and introduces variability, especially as device dimensions shrink to the nanoscale. Advanced techniques, such as metal gate technologies and high-k dielectrics, are needed to ensure performance at smaller nodes, which adds further challenges to scalability.

A significant issue in MuDFETs, particularly in nanoscale devices, is the self-heating effect, which can degrade performance and reliability. This thermal issue is more pronounced as transistors become smaller, and addressing it requires new materials with better thermal conductivity or advanced cooling solutions. In highly scaled transistors, SCEs, such as drain-induced barrier lowering (DIBL) and threshold voltage roll-off, pose significant problems. While MuDFETs like FinFETs and GAA FETs help mitigate SCEs, continued scaling below 5 nm will demand even more innovative approaches to control these effects. MuDFETs are prone to reliability issues, including bias temperature instability (BTI) and hot carrier injection (HCI), which can reduce device lifespan. These problems become more significant as the gate oxide thickness decreases, and solutions must focus on optimizing gate materials and interface engineering. The use of alternative materials, such as III–V compounds, has been proposed to improve carrier mobility in MuDFETs. However, integrating these materials into the existing silicon-based CMOS process poses compatibility issues, and the development of suitable deposition techniques is still in its early stages. The evolution of MuDFETs is moving toward novel structures such as stacked nanosheet FETs and vertical nanowire FETs. These architectures promise better electrostatic control and scalability compared to traditional FinFETs, potentially extending Moore's Law beyond current limits.

2D materials like TMDs and graphene offer high electron mobility and atomically thin channels, making them promising candidates for future MuDFET designs. However, challenges such as contact resistance and large-scale fabrication must be overcome before their practical use. TFETs, which leverage quantum tunneling for switching, are being explored to reduce power consumption in MuDFETs. TFETs promise subthreshold swings lower than conventional MOSFETs, making them ideal for low-power applications. However, achieving high performance at room temperature remains a challenge. As thermal management remains a critical bottleneck, integrating advanced materials with superior thermal conductivity, such as diamond-like carbon coatings or novel heat sinks, could be pivotal for future MuDFETs. These materials could help manage the thermal load in dense multi-gate structures. MuDFETs offer promising solutions to many of the challenges posed by device scaling. However, addressing fabrication complexity, improving material integration, managing thermal dissipation, and reducing device variability will be key to their success in future semiconductor technologies.

1.6 CONCLUSIONS

MuDFETs mark a substantial progress in semiconductor technology, engineered to tackle the scaling issues encountered by conventional planar transistors. By employing a multi-dimensional framework, MuDFETs improve current regulation, minimize leakage, and enhance overall performance, especially as device sizes decrease to nanometer dimensions. These transistors utilize a range of cutting-edge design techniques, such as 3D configurations and GAA designs, to optimize electrostatic control over the channel. MuDFETs provide various advantages, including reduced power usage, improved switching velocities, and greater scalability relative to traditional MOSFETs. Their multi-dimensional character enables superior suppression of SCEs, which are a significant limiting factor in traditional transistor designs as they reduce in size. This capability allows MuDFETs to sustain performance even in highly compact systems, making them ideal for contemporary applications in computing, communications, and other high-performance electronic devices. Nonetheless, the shift to MuDFET technology involves specific challenges. The manufacturing complexity is elevated due to the intricate shapes involved in these multi-dimensional designs. Furthermore, materials innovation, process integration, and cost efficiency are essential obstacles that need to be addressed to facilitate broad adoption.

In summary, MuDFETs signify a promising advancement in transistor technology, providing answers to the constraints of traditional devices. They have the potential to propel the next generation of electronic devices with their enhanced performance, scalability, and efficiency. While there are obstacles in their implementation, continuous research and development efforts are advancing the field, positioning MuDFETs as a crucial driver of future progress in semiconductor technology.

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2 Introduction to Multi-Dimensional Field Effect Transistors (FETs)

Piyali Saha

2.1 INTRODUCTION

Multi-dimensional field effect transistors (MDFETs) constitute a full-size evolution in semiconductor technology addressing the constraints of conventional planar FETs because the enterprise sends toward smaller extra green and better-appearing gadgets. Traditional field-effect transistors (FETs), such as metal-oxide-semiconductor FETs (MOSFETs), face significant challenges as device dimensions scale down. These issues include increased leakage currents and pronounced short-channel effects, which arise due to reduced transistor sizes. To overcome those demanding situations, MDFETs consisting of FinFETs and gate-all-around FETs (GAA FETs) were developed. FinFETs feature a thin, fin-like structure extending from the silicon substrate, allowing the gate to wrap around three sides of the channel. This design enhances electrostatic control, reduces leakage, and improves overall device performance. Gate-All-Around (GAA) FETs advance this concept further by completely surrounding the channel with the gate, offering superior control and making them well-suited for advanced, scaled-down technology nodes. Additionally, nanowire and nanosheet FETs variants of GAAFETs provide the ability for further miniaturization and Productivity gains. The improved gate control in planar FETs results in lower power consumption, making them ideal for applications requiring efficient data transmission, such as flexible electronics, IoT devices, and high-performance computing where processing power is critical. However, these advanced architectures also present challenges, including increased fabrication complexity and the need for better materials and thermal management solutions. As the semiconductor industry continues to scale down devices, planar FETs are expected to play a crucial role in sustaining Moore's Law, enabling advancements in emerging technologies like quantum computing, artificial intelligence, and next-generation processing systems. Despite the hurdles the adoption of MDFETs is decisive for the continued advancement of electronics offering a pathway to more powerful efficient and compact devices.

2.1.1 MOORE'S LAW

Gordon Moore introduced the now-famous Moore's Law in 1965. It states that a chip's transistor density will double every 2 years [1]. This rule has held true for over 50 years driving the creation of devices like smartphones and computers.

DOI: 10.1201/9781003543923-2

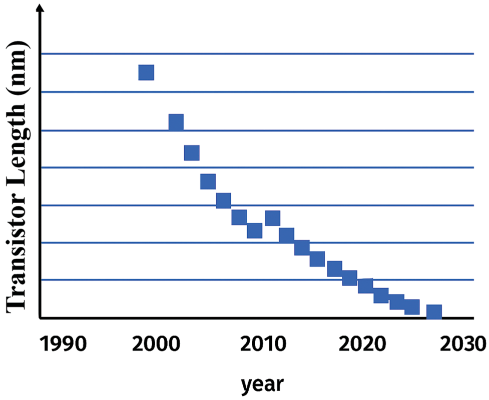

FIGURE 2.1 Moore's theory, illustrating the number of transistors on a chip versus the years, the transistors quantity fabricated on a chip multiplies. This graph depicts the best probable situation through 2030.

From Figure 2.1, to keep up with this law, engineers need to shrink transistor sizes. This allows silicon wafers of the same size to fit more transistors boosting the chip's capabilities. But Moore's Law isn't just about doubling transistor count. It also predicts a decrease in transistor costs and a boost in transistor performance. One way to achieve this is to speed up the chip's processing while cutting down on its power use.

Currently, more than 2.5 trillion MOSFET may be arranged on a silicon wafer [2], a doubling of the transistor count, but it also necessitates a drop in the price and enhancement in each transistor efficiency.

2.1.2 SHORT-CHANNEL EFFECT

As MOSFET sizes have been continuing to shrink in recent years, a number of associated issues have surfaced along with growing technological difficulties. The one that affects the chip's functionality the most is the short-channel effect. The MOSFET starts to show signs of rising off-state current as its channel gets shorter and shorter [3,4]. This indicates that even though the gate voltage is used to inhibit current flow, certain carriers are still able to travel freely across the source and drain. Specifically, the electric field at the drain end of the channel increases as the channel length, l, is reduced, making it more probable that an electron can tunnel through the oxide layer and reduce the effective channel length. This causes a rise to the threshold voltage and drop in the drain current that can be detrimental to transistor performance and result in energy inefficiencies. The typical functioning and efficiency of MOSFETs are greatly impacted by the short-channel effect as shown in Figure 2.2 [5]. As a result, the Moore's Law estimate has been updated by the International Technology Roadmap for Semiconductors (ITRS) from twice the number of MOSFETs every 2–4 years to every 3 years. Currently, there are essentially two approaches to address the short-channel effect. One is to alter the semiconductor material used in MOSFETs.

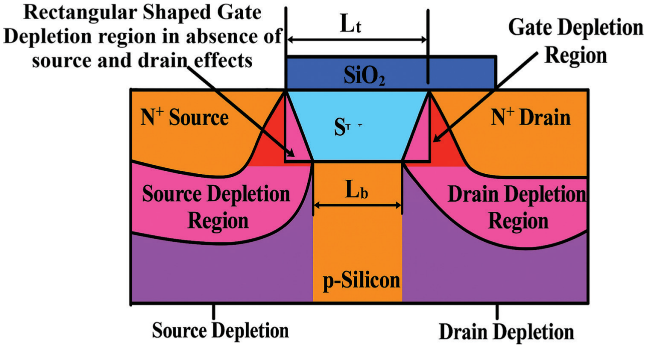
Rectangular Shaped Gate Depletion region in absence of source and drain effects
L_t
Gate Depletion Region
SiO_2
N^+ Source
S_T
N^+ Drain
Source Depletion Region
L_b
Drain Depletion Region
p-Silicon
Source Depletion
Drain Depletion

FIGURE 2.2 Short-channel effects in metal oxide semiconductor field effect transistors (MOSFETs).

2.1.3 EVALUATION OF MULTI-DIMENSIONAL FET

These MDFETs can be assessed in terms of performance, advantages, drawbacks, and possible ergonomic applications. Here is a tabulated assessment of it [6].

i. **Improved Transistors' Control and Performance**: Multi-gate FETs include Fin Field Effect Transistors (FinFETs) and nanowire FETs, whose advantage against planar FETs is enlarged gate control because of improved electrostatic control, reduced leakage currents, and superior switching characteristics.
ii. **Higher Packing Density of Devices**: These would facilitate higher packing densities by the use of multiple gates or dimensions, hence enabling more transistors per unit area [7]. This is a key method to make electronic devices smaller while keeping or increasing performance.
iii. **Better Device Speed and Efficiency**: MDFETs have lower switching speeds compared to their planar counterparts, but this class in general will have lower speeds of switching and power consumption to yield a performance comparable to that of other devices. This in turn would mean they are better for applications involving high-speed computing, portable devices, and those requiring power sensitivity for efficiency.
iv. **Device Variety and Performance**: The ability to create a transistor with multiple switches or gates allows configurations that are very adaptable because of this versatility and flexibility, and provides opportunities for innovation in implementing circuits that use logic, memory, sensing, and other integrated technologies.
v. **Beyond CMOS Applications**: Multi-dimension FETs make way for post-CMOS technology, with the ability for singular quantum advances, neuromorphic computing, or any other progress in implementing the new ways to control or switch electrical signals [8].

Multi-dimensional transistors face several hurdles:

i. **Tricky Manufacturing**: MDFETs needs cutting-edge tech like nanolithography and exact material layering. This can be pricey and might run into snags with consistency and reliability across devices.
ii. **Scaling Issues**: As things get smaller to boost speed, keeping everything uniform and limiting differences get harder. Tweaks in how they're made can change transistor features and hurt how well the whole device works.
iii. **Heat Problems**: Packing more into less space can make more heat. This means dealing with heat is key to stop bad overheating and keep things running [9].
iv. **Material Mix and Match**: Using different stuff to make transistor parts, like various semiconductors for gates, brings up questions about how well they work together. It's crucial to make sure everything fits well and works across materials.

MDFETs, including planar and non-planar architectures, are highly suited for high-performance computing (HPC) applications that demand fast processing and high integration density. They enhance processing speed while consuming less power, improving overall computing efficiency. In portable electronics and IoT devices, these FETs extend battery life and boost processing performance. Their efficient energy handling also makes them ideal for energy-sensitive applications. Additionally, MDFETs enhance sensor performance by integrating multiple sensing elements, benefiting fields like healthcare monitoring, environmental sensing, and industrial automation. Beyond conventional uses, they play a crucial role in emerging technologies such as quantum computing and neuromorphic (brain-inspired) systems. Their unique properties enable compact, efficient, and scalable designs, making them essential for the advancement of modern and future electronics [10]. Overall, MDFETs offer significant improvements in performance, miniaturization, and versatility, positioning them as key enablers of next-generation computing.

2.2 PHYSICS OF MULTI-DIMENSIONAL FET

The physics of MDFETs entails comprehending how the multi-gate or multi-channel architecture of the transistor affects its characteristics and mode of operation [11]. The fundamental ideas of physics at play are as follows:

2.2.1 Gate Control and Electrostatics

Many gates or pathways are used to control the current across the transistor in MDFETs, including both FinFETs and nanoscale FETs [12]. The basic principles of gate control are outlined very briefly here:

i. **Gate Capacitance**: The capacitance of the gate of all inducing effects has on the channel electronically. A gate voltage, V_G, attracted or repelled carriers of charge (electrons or holes), which altered the conductivity of the channel and controlled current flow.

ii. **Threshold Voltage (V_th)**: The electrostatics at the gateway channel interface determine the threshold voltage at which the transistor changes state from off to on. MDFETs nowadays tend to have steeper subthreshold slopes because of superior gate control, which brings a high switching efficiency and lowers the leakage currents.

2.2.2 CHANNEL CONDUCTIVITY AND MOBILITY

i. **Carrier Transport**: Two mechanisms which can transport the carriers are drifting and diffuse, and they depend on the nature of semiconductor material used in the channel silicon, III-V materials, or nanowires [13]. The mobility and general effectiveness of the transistor depend on channel width and the quality of its material, such as carrier mobility.
ii. **Quantum Effects**: For FETs, in nanotechnology, quantum mechanical effects are significant. Six quantum entrapment influences carrier density, amount of energy, and transport properties in multi-gate designs for nanowires or quantum wells.

2.2.3 SCALING AND DIMENSIONAL EFFECTS

i. **Gate Length and Width**: It directly relates to performance measurement concerning speed, power, and leakage current in transistors. As gate length gets reduced, it allows higher packing densities and faster switching speeds while resulting in more complex manufacturing and variability management.
ii. **Short-Channel Effects**: Reducing the gate length aggravates the short-channel effects, which cause subthreshold-slope degradation and drain-induced barrier lowering. MDFETs alleviate the degradation caused by these effects due to a decrease in channel electrostatics and an enhancement of the gate control [14].

2.2.4 THERMAL AND NOISE CONSIDERATIONS

i. **Waste Heat Generation**: MDFETs of higher integrated densities can generate more heat per surface area, and maintaining device reliability and efficiency in highly power-consuming applications is in urgent need of thermal control.
ii. **Noise Performance**: Noise insulation and sensitivity are directly affected by the size of gate and channel. MDFETs can perform better regarding noise due to their better gate control and reduced extraneous capacitances.

2.2.5 ADVANCED MATERIALS AND INTERFACES

i. **Heterostructures and Interfaces**: Most MDFETs include heterostructures in which different semiconductor materials are integrated together to achieve the best carrier transport and performance of devices. The interface between these different materials will be very critical in a MDFET for determining the characteristics of the transistor and its reliability [15].

2.3 MULTI-DIMENSIONAL FET STRUCTURE

MDFETs are basically different in shape compared to conventional planar FETs by incorporating a couple of gates or channels. The following is the fashionable overview of systems generally seen in MDFETs.

2.3.1 FinFET Structure

FinFET serves as a 3D transistor in today's integrated circuits. It has evolved from the standard MOSFET and plays a key role in cutting-edge semiconductor processes (such as 14 nm, 10 nm, 7 nm, and tinier) [16]. The design of FinFET enables enhanced channel management, which cuts down on leakage current and boosts performance as transistors get smaller. Cross-sectional view of FinFET structure is shown in Figure 2.3.

2.3.1.1 Features of FinFET Structure

i. **3D Structure**: In contrast to old-school flat transistors with channels lying on silicon bases, FinFETs sport raised channels nicknamed "fins." This design lets manufacturers control the channel from several angles boosting electrical performance.

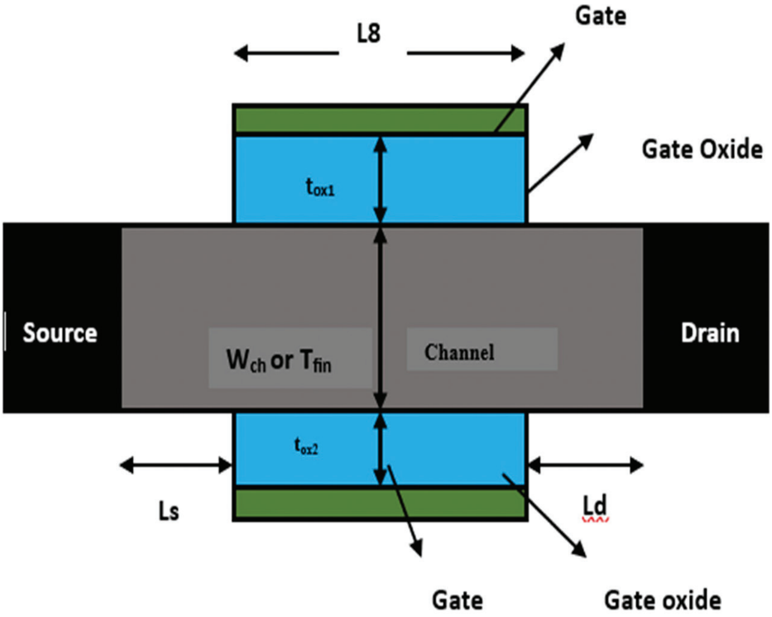

FIGURE 2.3 Cross section of fin field effect transistor (FinFET).

ii. **Gate Control**: FinFET gates hug the fin (the channel) on three sides: the top and both sides [17]. This setup gives better control over the channel's electrics, which helps cut down on short-channel effects that pop up in tinier transistor sizes.
iii. **Reduced Leakage Current**: A key perk of FinFETs is that they slash leakage current (subthreshold leakage), which becomes a big headache in smaller process nodes. The enhanced gate control helps keep this leakage in check.
iv. **Scalability**: FinFETs have better scalability than standard planar transistors, which allows their use in smaller tech nodes [18]. This plays a key role as the industry shifts to tinier transistor sizes leading to higher density and improved performance in chips.
v. **Fin Pitch and Width**: The quantity of fins and their measurements impact the transistor's drive strength. Putting multiple fins in parallel can boost the device's ability to carry current.

2.3.1.2 FinFET Key Components

i. **Fin**: The slim upright silicon structure that acts as the channel between the source and drain.
ii. **Gate**: Wraps around the fin on three sides (top and two sides) to manage the current flow through the fin.
iii. **Source and Drain**: Sit at opposite ends of the fin. The source puts carriers into the channel, while the drain gathers them.

2.3.2 GAA FET STRUCTURE

The GAA FET is another evolution in the next step over FinFETs in advanced transistor architecture, enabling even better control of the channel for improved scaling semiconductor technology nodes. Notably, it is considered that GAA FETs as shown in Figure 2.4 play a significant role in moving beyond the 5 nm process node.

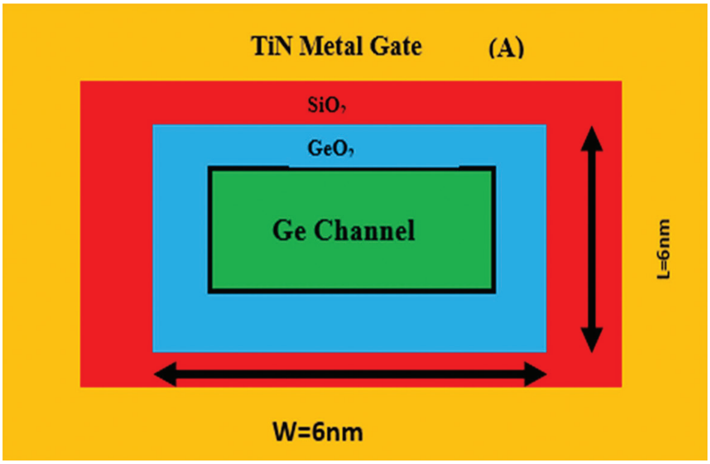

FIGURE 2.4 Gate-all-around field effect transistors (GAA FET).

2.3.2.1 Features of GAAFET Structure

1. **Surrounding Gate**: GAA FETs differ from FinFETs, in which the gate surrounds the channel on three sides, with the former surrounded on all sides by the gate. This allows for better electrostatic control of the channel, which reduces short-channel effects and leakage currents.
2. **Nanosheet or Nanowire Channel**: The channel in GAA FETs is of a nanosheet or nanowire structure [19]. In this respect, the nanosheets are arranged horizontally, while the gate is wrapped around each nanosheet, resulting in even far superior gate control compared to previous FinFETs.
3. **Improved Scalability**: GAA FETs are projected to scale down even to 3 nm and below, which is considered vital for continuing Moore's Law. In such minute-scale settings, the architecture offers tight control over the device characteristics.
4. **Less Leakage**: Improved gate control in GAA FETs further reduces leakage currents over FinFETs.
5. **Flexible Channel Dimensions**: This is achieved through changing the width of the nanosheets to reach the proper performance–power trade-off [20]. Wider nanosheets support higher drive currents, whereas narrower ones can be used in cases where power consumption must be reduced.

2.3.2.2 GAAFET Key Components

1. **Nanosheet or Nanowire**: Thin, ribbon-like or wire-like channels in which the current will flow. The nanosheets or nanowires can be additional stacked vertically to make a drive stronger.
2. **Gate**: The gate completely surrounds each nanosheet or nanowire, enabling ultimate control of the channel.
3. **Source and Drain**: One end point of the nanosheets/nanowires; a point at which carriers are injected and collected.

2.3.3 OTHER MULTI-DIMENSIONAL CONFIGURATIONS

Beyond FinFETs and GAAFETs

1. **Multi-Bridge Channel FETs**: Multiple independent conducting channels are bridged over by gates for better current and low-resistive handling. Figure 2.5 depicts the 3D view of Multi-Bridge Channel FETs.
2. **Nanowire FET**: Nanowires serve as the individual conducting channel(s) of the transistor and are typically composed of semiconductor materials like silicon, III-V compounds, or even carbon nanotubes. The cross-sectional view of nanowire FET is shown in Figure 2.6. Nanowire FETs can consist of several gates that can be placed on the circumference or along the length of the nanowires to control the flow of current through the nanowire channel. Nanowire FETs, like the FinFETs, possess a dielectric layer that aids in isolating and controlling the gate and nanowire channel [21].

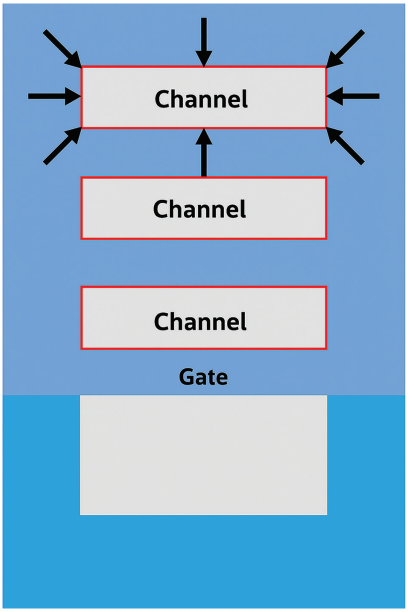
Channel
Channel
Channel
Gate

FIGURE 2.5 Multi-bridge channel metal oxide semiconductor field effect transistor (MBCFET) structure.

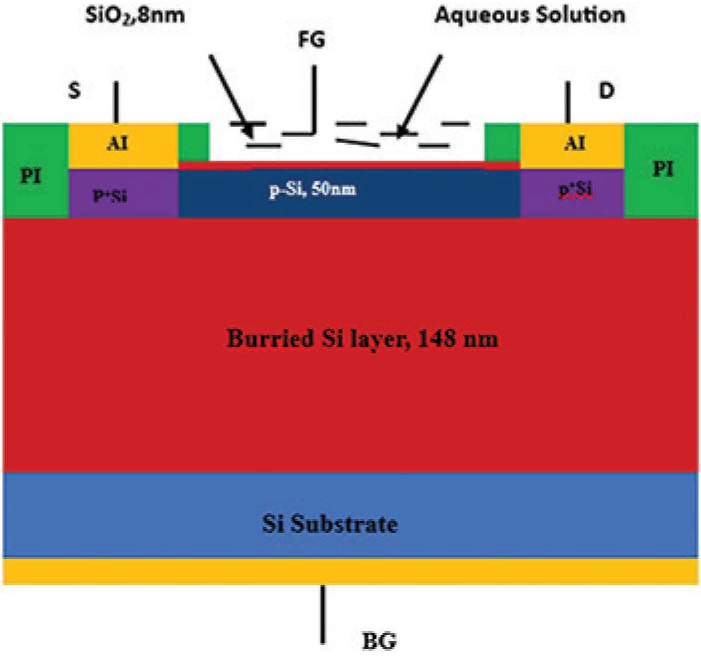
SiO₂,8nm
Aqueous Solution
FG
S
D
Al
Al
PI
PI
P+Si
p-Si, 50nm
p+Si
Burried Si layer, 148 nm
Si Substrate
BG

FIGURE 2.6 Nanowire field effect transistor (FET) structure.

2.3.4 Applications and Future Directions

MDFETs are going to be significant in improving the associated semiconductor technology:

i. **Applications**: This has very important high-performance computing, mobile, and IoT sensor technology succubae, and this is a big thing to consider in quantum computing advancement also.
ii. **Prospects**: Current research focuses on material integration, further miniaturization of device dimensions, and exploration of new architectures to make future electronics a reality.

The proper understanding of these structures is essential for the development and optimization of MDFET designs for the requirements of many applications in current-day electronic systems.

2.4 TYPES OF MULTI-DIMENSIONAL FET

Very interesting varieties that have been developed to be based on different structural configurations and principles of operation are MDFETs. Some common types of MDFETs are listed below.

2.4.1 FinFET (Fin Field Effect Transistor)

2.4.1.1 FinFET Structure

A FinFET is a sort of three-dimensional transistor; these upgrades have improved both the performance and power efficiency of advanced integrated circuits. While traditional planar transistors possess a flat channel, in a FinFET, a thin vertical silicon "fin" serves as the channel. This fin is wrapped on three sides by the gate, hence giving a finer control of electron flow [22]. Figure 2.7 depicts the cross-sectional view of FinFET structure.

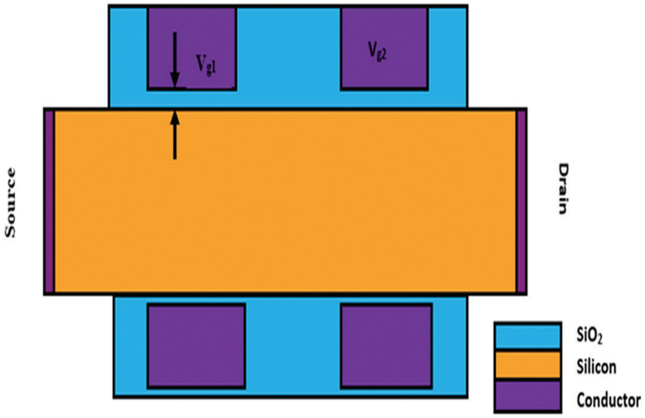

FIGURE 2.7 Fin field effect transistor (FinFET) structure.

This 3D structure reduces the leakage currents and allows for higher switching speed, thereby making FinFETs more efficient compared to their planar counterparts [23]. They are very essential in extending Moore's Law because these perform well at smaller process nodes, for example, 14 nm and below. These find wide applications in leading-edge processors, GPUs, and SoCs that will enable advanced and power-efficient electronic devices.

FinFET technology is one of the major leaps in the evolution cycle of transistors, in which most of the issues with which conventional transistors chose to live—for instance, channel control, leakage current, and scalability—have been solved [24]. For this reason, FinFETs are important parts in the development process for producing small-size, fast, and power-efficient electronic gadgets.

2.4.1.2 Advantages

i. **High-Performance**: FinFETs can operate on better switching speed and drive strength; the latter provides better overall performance in integrated circuits.
ii. **Lower Power Consumption**: FinFETs have less leakage and give better control over the channel, hence consuming less power. This advantage makes FinFETs perfect for mobiles and other low-power devices [25].
iii. **Increased Density**: The 3D nature enables more transistors in a given area, and this feature is a must to make smaller and powerful chips.

2.4.1.3 Applications

i. **Microprocessors**: High-performance microprocessors use FinFETs to increase the speed at which they switch on and off, hence increasing their processing capabilities. Their efficiency at lower node size allows them to realize faster, stronger processors.
ii. **Graphics Processing Units (GPUs)**: FinFET technology is used by GPUs in order to interface with the complex, high-speed graphic processing. It helps raise the bar of general performance and lower power consumption for rendering high-resolution images and videos.
iii. **System-on-Chips**: The most important thing in SoCs used in smartphones, tablets, and other portable devices, FinFETs have made a way for improving energy efficiency and performance that are crucially needed to handle multitasking on devices by saving battery life.
iv. **Memory Devices**: Advanced memories, such a static random access memory (SRAM) and dynamic random access memory (DRAM), employ FinFETs for speed improvement with lower power consumption. The performance improvement therefore allows faster access to data and lower energy consumption in memory chips.
v. **Networking and Data Centers**: FinFETs were used in data centers and networking equipment for high-speed data processing, with better power consumption for more volumes of data transfer and maintaining energy efficiency.
vi. **Consumer Electronics**: Laptops, ultra-books, tablets, and smartphones use FinFET technology for a leap in performance with long battery life.

The technology provides overall efficiency of the device and increases users' experiences.

vii. **Automotive Electronics**: Automotive electronics use FinFETs for high-reliability and performance applications such as ADAS and infotainment. Power efficiency is also important for electric and hybrid vehicles.

2.4.2 NANOWIRE FET (NWFET)

2.4.2.1 Structure

A nanowire FET is a class of advanced transistor where the flow of current takes place through a nanometer-scale wire. This nanowire can be made with materials such as silicon or other semiconducting materials. Typically, the nanowire surrounds the gate, hence offering excellent control over the channel [26]. Compared to a traditional planar or FinFET design, GAA nanowire FETs have a better structure in terms of electrostatic control, providing leakage current reductions by an order of magnitude and improvements at very small scales. For scaling semiconductor technology down to 5 nm and beyond, enabling more powerful energy-efficient electronic devices, nanowire FETs are extremely critical. Figure 2.8 depicts the cross-sectional view of 2D nanowire FET structure.

2.4.2.2 Advantages

i. **Superior Electrostatic Control**: The nanowire FET GAA structure allows the gate to be totally encapsulating the nanowire channel, allowing great control over the conductivity of the channel. This suppresses short-channel features and leakage currents—major concerns with the scaling down of transistor dimensions.

ii. **Scalability**: The scalability of nanowire FETs is excellent; hence, they are performing extremely well for very small process nodes, such as below 5 nm. Therefore, they are fit for further scaling in the semiconductor device toward the satisfaction of Moore's Law.

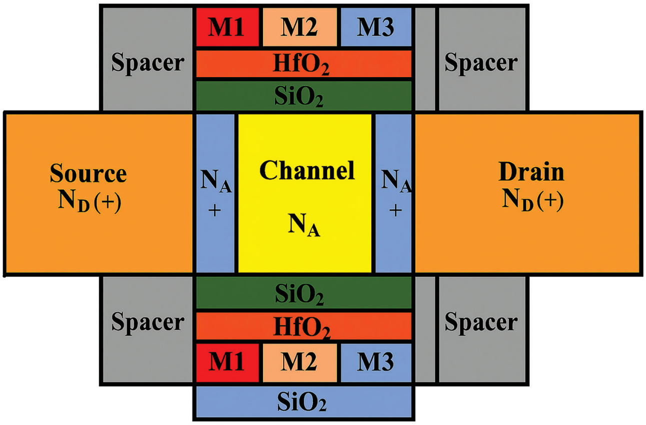

FIGURE 2.8 Cross-sectional view of 2D nanowire field effect transistor (FET).

iii. **Enhanced Performance**: Because of improved channel control, nanowire FETs can increase the speed of switching and reduce power consumption, which helps to improve overall performance in integrated circuits.
iv. **Flexibility in Design**: That can be optimized in diameter and length with respect to the transistor design for different applications, hence making an optimal balance between drive current and power efficiency [27].
v. **Leakage Current Is Reduced**: The GAA structure minimizes leakage currents in nanowire FETs, and therefore, this gives the nanowire FETs the prospect of being more power-efficient, especially in low-power and mobile devices.

2.4.2.3 Applications

i. **Advanced Microprocessors**: The scalability and performance improvement of nanowire FETs are the major reasons behind the introduction of the latest generation microprocessors. These are in view of realizing improved computational powers and energy efficiencies.
ii. **Memory Devices**: Their application is realized in advanced memory technologies like SRAM and DRAM, with reduced leakage and fast switching, which are key factors toward high-performance memory.
iii. **Low-Power Electronics**: Due to their low power consumption, nanowire FETs are ideal for a wide range of applications in mobile electronics, wearable electronics, and IoT.
iv. **High-Frequency Applications**: Nanowire FETs are also suitable for high-frequency applications such as radio frequency (RF) transceivers and millimeter-wave circuits owing to fast switching.
v. **Next-Generation Semiconductor Devices**: As semiconductor technology continues its evolutionary path, nanowire FETs may express a fundamental role in conduction for next-generation devices toward further miniaturization and improved performance of electronic systems.

2.4.3 NANOSHEET FET (NSFET)

2.4.3.1 Structure

A nanosheet FET is a more advanced new transistor technology being implemented with a view to further improving performance and efficiency of power in semiconductor devices. The structure of the NSFET consists of a stack of thin horizontal nanosheets composed of semiconductor material such as silicon or other advanced materials. Figure 2.9 shows the cross-sectional view of nanosheets, which act like a channel through which the current flows, with the gate wrapping around each nanosheet to ensure great electrostatic control. In this respect, GAA configuration provides a better suppression of leakage currents and an improvement in channel control compared with traditional planar or FinFET designs [28]. The stacking of many nanosheets allowed in NSFETs provides the possibility for high drive current and efficient scaling to smaller process nodes, hence becoming one of the strong solutions for technological advancements in fields of high-performance and low-power applications.

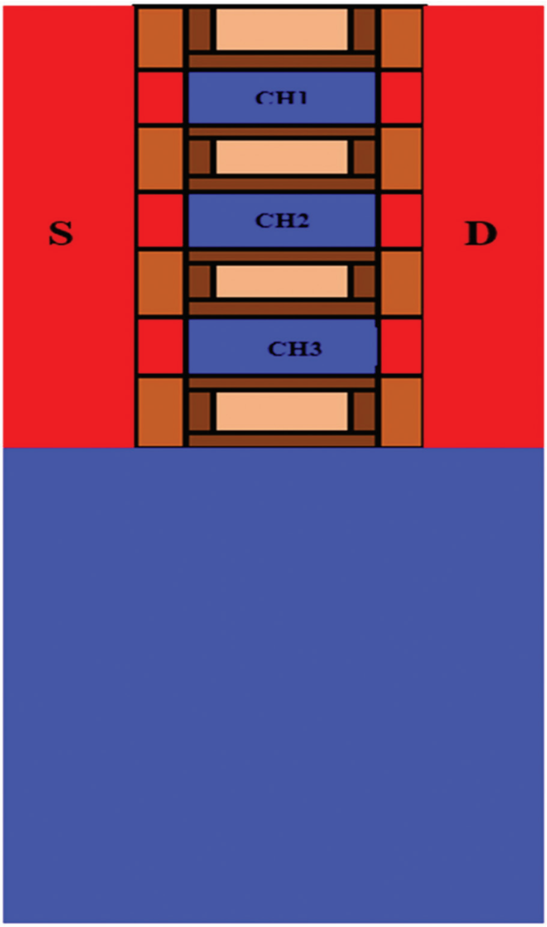

FIGURE 2.9 Cross section of nanosheet field effect transistor (FET) structure.

2.4.3.2 Advantages

i. **Better Electrostatic Control**: It helps in better control of the channel, as the GAA structure in NSFETs wraps the nanosheets totally. This reduces short channel effects (SCEs) and leakage currents very effectively, which is very much essential for maintaining performance at reduced transistor sizes.
ii. **High Drive Current**: Due to increased stacking in nanosheets, NSFETs are able to drive current with a very significant increase. This directly translates into higher performance with better efficiency for high-speed applications that require high performance.
iii. **Improved Power Efficiency**: NSFETs would have lower leakage currents, and thereby, better electrostatic control, leading to lower power consumption. This is important not only for energy-efficient computing but also for battery-powered applications [29].

iv. **Scalability**: Because of the nanosheet structure, NSFETs can be scaled down to very small nodes of the process at 3 nm and below; this architecture is suitable for future generations of semiconductor technology, extending Moore's Law.

v. **Design Flexibility**: The width and number of stacked nanosheets can be optimized with respect to the application of the transistor, which allows a proper balance between performance and power consumption by designers.

2.4.3.3 Applications

i. **Microprocessors**: NSFETs are applied to high-performance microprocessors, hence fast processing speed and improved power efficiency. Being competent in handling complex computations, they present themselves as suitable for advanced computing applications.

ii. **Graphics Processing Units (GPUs)**: In GPUs, NSFETs lead to higher performance and efficiency both in terms of rendering high-resolution graphics and parallel computation, which tunes up the graphical performance further.

iii. **System-on-Chips (SoCs)**: NSFETs are adopted in SoC based on the performance, low power consumption for smartphones, tablets, and other integrated devices. This helps improve functionality and battery life in these devices.

iv. **Memory Technologies**: Advanced memory devices are tending toward NSFET technology because of the fast access speed and low power consumption, which is very vital for HPC and data storage.

v. **Wearable and Portable Electronics**: The main performance of wearable devices and other portable electronics is a trade-off in NSFETs for battery lifetime, and thus, it is suitable for compact and energy-efficient design.

vi. **Data Centers and Networking Equipment**: Data centers and networking equipment consume large volumes of data with minimal operational costs, which is an important usage enabled by NSFETs for high-speed data processing energy efficiency.

2.4.4 MULTI-BRIDGE CHANNEL FET (MBCFET)

2.4.4.1 Structure

An MBCFET, as shown in Figure 2.10, is a heightened concept in designing transistors where there are several bridges on one transistor to enhance performance and increase power efficiency. By structure, an MBCFET contains a core transistor with a number of parallel bridges of semiconductor material connecting source and drain regions; these bridges are integrated within a configuration known as a GAA structure, the gate surrounds the entire channel, thus allowing superior electrostatic control. It also reduces short-channel effects and leakage currents, enabling higher drive currents. The multi-bridge approach enhances the transistor capability for handling high-speed switching and makes MBCFETs quite suitable for microprocessors of next-generation, memory devices, and HPC systems [30].

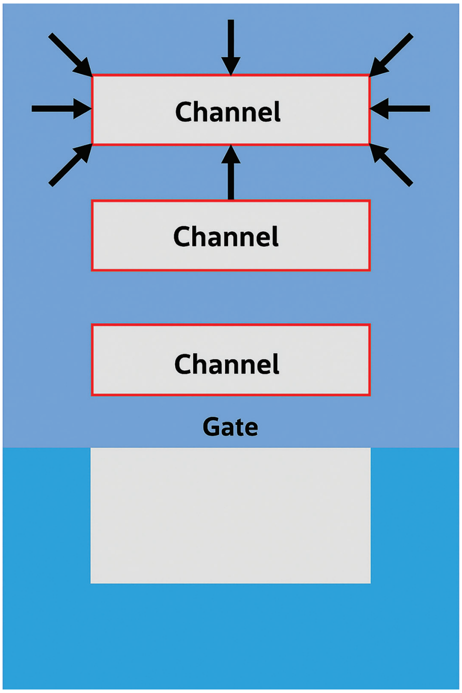

FIGURE 2.10 Multi-bridge channel field effect transistor (MBCFET) structure.

2.4.4.2 Advantages

i. **Improved Drive Current**: Large effective channel width and the possibility to implement higher drive currents are enabled by multiple parallel bridges within one MBCFET design. This would mean better performance for high-speed and high-power applications.
ii. **Superior Electrostatic Control**: The multi-bridge design further supports the GAA structure of MBCFETs in providing excellent electrostatic control of the channel, reducing short-channel effects and leakage currents, adding to overall transistor efficiency.
iii. **Improved Performance and Power Efficiency**: MBCFETs have shown a good balance between high performance and low power. With better drive current and reduced leakage, the device becomes more power-efficient. This is an important requirement for modern-day electronics.
iv. **Scalability**: The MBCFET structure will scale down to smaller nodes that can support continued advancements in semiconductor technology. It will help maintain performance improvements with shrinking transistor sizes [31].
v. **Flexibility in Design**: The multi-bridge approach offers flexibility in the optimization of the transistor for specific applications by adjusting the number and configuration of bridges. This allows great tuning of performance characteristics, based on application needs.

2.4.4.3 Applications

i. **High-Performance Microprocessors**: MBCFETs find their applications in advanced microprocessors that switch faster, hence offering greater computational power suitable for demanding computations.
ii. **Graphics Processing Units (GPUs)**: In the case of GPUs, MBCFETs would improve performance by enabling high-resolution graphics and executing complex algorithms, thereby increasing graphical and computational efficiency.
iii. **System-on-Chips (SoCs)**: High-performance MBCFETs are being increasingly used in SoCs targeted for leading performance and energy efficiency, so important for smartphones and other advanced tablets and integrated devices. It finds increasing usage, especially in leading-performance and energy-efficient SoCs targeted for smartphones and other advanced tablets and integrated devices [32].
iv. **Memory Devices**: Advanced memories, including SRAM and DRAM, place the MBCFETs well with their enhanced performance–power efficiency in applications that need very high data access speed and ultralow power.
v. **Data Centers and Networking Equipment**: MBCFETs enable data processing at high speed and with low power consumption in data centers and networking equipment. That makes operating easier with huge volumes of data, while operational efficiency remains the same.

2.4.5 TRI-GATE FET (3D FINFET)

2.4.5.1 Structure

The so-called tri-gate FET is an evolutionary leap beyond the conventional planar MOSFET. Its vertical fin-shaped semiconductor channel rises from the silicon substrate, its gate wrapping around the fin on three sides—the top and the sidewalls. This three-dimensional gate configuration allows for much better electrostatic control over the channel, hence enhancing toaster capability in managing leakage currents and improving the speed of switching [33]. The extended gate coverage in tri-gate FET reduces short-channel effects, enabling superior performance and energy efficiency with scaled-down process nodes. This will become increasingly important in maintaining miniaturization on semiconductor devices while increasing power performance. Figure 2.11 depicts the cross-sectional view of tri-gate FET structure.

2.4.5.2 Advantages

i. **Improved Electrostatic Control**: Because, in the tri-gate FETs, the gate wraps around the fin on three sides, offering superior control over the channel. This reduces the short-channel effects and leakage currents, hence enhancing the efficiency and performance of the transistor.
ii. **Improved Performance**: The 3D structure allows better current drive and faster switching speeds compared to traditional planar MOSFETs. Consequently, this improves the overall performance of integrated circuits [34].

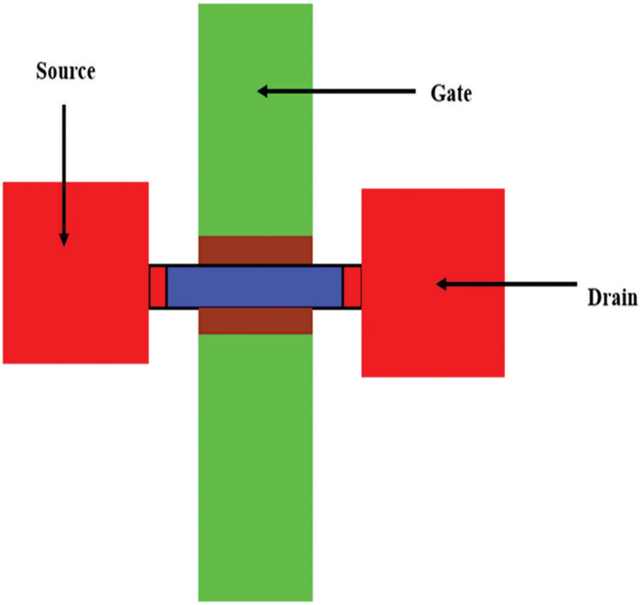

FIGURE 2.11 Tri-gate field effect transistor cross-sectional view.

iii. **Lower Power Consumption**: Tri-gate FETs minimize power consumption by minimizing leakage currents and increasing electrostatic control. This is considered extremely important in enabling energy-efficient electronic devices, especially in mobile and portable applications.

iv. **Scalability**: Tri-gate FETs continue functioning well at smaller process nodes, such as 22, 14, and 10 nm, hence further scaling semiconductor technology. This three-dimensional structure allows higher transistor density and better performance in smaller chip designs.

v. **Reduced Short-Channel Effects**: Where the vertical fin structure reduces the short-channel effects associated with the shrinking of transistors to ensure reliable performance even with the reduction in size.

2.4.5.3 Applications

i. **Microprocessors**: Tri-gate FETs make the bigger brother of high-performance microprocessors and achieve faster processing speeds with more computational power. While doing so, the latter is suitable for higher computing tasks and applications.

ii. **Graphics Processing Units (GPUs)**: In GPUs, tri-gate FETs improve performance for complex graphics rendering and parallel processing tasks; therefore, they help in graphics performance and efficiency.

iii. **System-on-Chips (SoCs)**: Tri-gate FETs are found in SoCs for smartphones, tablets, and other integrated gadgets. The energy efficiency and performance benefits are quite significant to the balance required between power consumption and computational needs [35].

iv. **Memory Devices**: Advanced memories, such as SRAM and DRAM, utilize tri-gate FETs—a way to enhance performance with ultimate device speed and lower power dissipation, which plays a significant role in storing and accessing data at high speed.

v. **Consumer Electronics**: Enhanced performance along with long battery life can be witnessed in laptops, tablets, and smartphones due to tri-gate FETs, making users more productive and efficient with their devices.

vi. **Data Centers**: These tri-gate FETs have helped enable high-speed data processing with energy efficiency in the data centers to feed the voracious demand for both data handling and computational power.

2.4.6 GAA FET

2.4.6.1 Structure

The advanced GAA transistor is a fully enclosed FET that is shown in Figure 2.12 to surmount the threshold of conventional planar and FinFET transistors. In the GAA FET, the gate completely wraps around the semiconductor channel on all sides—like top and both sidewalls—thus making it a full 3D structure. This allows for superior electrostatic control over the channel, with significantly reduced leakage currents and hence improved performance. The channel material can be in the form of nanosheets or nanowires for the GAA FET, which can be stacked to drive the current higher and sustain high performance at smaller process nodes [36]. This architecture further allows for superior efficiency and scalability of the transistor, besides advancing the wheels of progress in semiconductor technology to enable more compact, high-performance, and energy-efficient electronic devices.

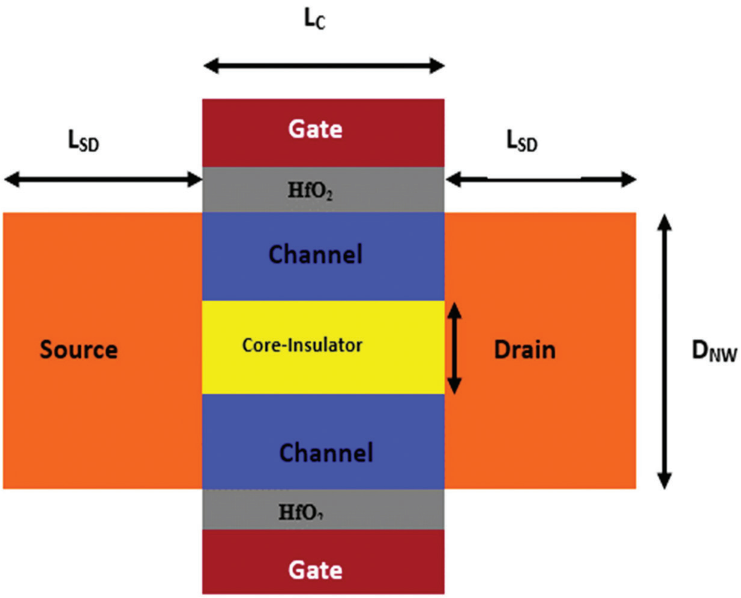

FIGURE 2.12 The overall dimension of gate-all-around field effect transistor.

2.4.6.2 Advantage

i. **Superior Electrostatic Control**: In the case of GAA FET, the gate wraps around the entire channel and hence has phenomenal control over the flow of electrons. This reduces short-channel effects and leakage currents, thus giving way to improved performance and efficiency.

ii. **Higher Performance**: The fact that the gate fully surrounds the channel means both the current that can be driven through and the time taken for switching are increased manifold in GAA FETs, which directly translates to better overall performance in high-speed applications.

iii. **Reducing Leakage Current**: The comprehensive gate control reduces the leakage currents. Hence, low power consumption becomes achieved, which becomes important in implementations where devices should have battery power and be energy-efficient.

iv. **Scalability**: Generally speaking, GAA FETs scale down more to smaller process nodes when dealing with conventional planar or FinFET transistors. Thus, this device is better positioned for the next generation of semiconductor technology development in further shrinking of devices [37].

v. **Flexibility in Design**: Therefore, the GAA architecture will be enabled with various channel materials and structures—nanosheets and nanowires—to allow optimization for performance and power requirements.

2.4.6.3 Applications

i. **Advanced Microprocessors**: GAA FETs find their application in high-performance microprocessors, which provide higher computational power and efficiency, hence rendering them appropriate for complex and demanding computations.

ii. **Graphics Processing Units (GPUs)**: In GPUs, GAA FETs avail higher rendering power of high-resolution graphics, while in intensive parallel computation, this device contributes to higher graphical and processing power.

iii. **System-on-Chips (SoCs)**: The GAA FETs find their application in SoC for smartphones, tablets, and other integrated devices where its high performance and low power consumption benefit both processing and battery life.

iv. **Memory Devices**: Advanced memory technologies like SRAM and DRAM utilize GAA FETs for higher access speeds with lower power consumption to store and retrieve data efficiently [38].

v. **Wearable and Portable Electronics**: GAA FETs find their use in wearables and portable devices, balancing high performance with long battery life, thus making compact and power-efficient designs possible.

vi. **Data Centers**: GAA FETs address the issues of speeding up data processing and energy consumption in data centers with thoughtful consideration of high-volume data management and cost efficiency.

2.4.7 APPLICATIONS AND FUTURE DIRECTIONS

The diverse range of MDFET variants will play a pivotal role in advancing the semiconductor era across multiple application domains. In high-performance computing (HPC), they enable faster processing and greater efficiency. In mobile and IoT devices, they support low-power operation while offering enhanced functionality. For emerging technologies, these FETs provide the foundation for breakthroughs in areas such as quantum computing and neuromorphic computing, among others. Each type of MDFET has its own unique advantages, based on specific performance metrics, which render them important components in the course of the evolution of electronics and computing methods [39].

2.5 CHALLENGES AND IMPROVEMENTS OF MULTI-DIMENSIONAL FET

2.5.1 Challenges of Multi-dimensional FET

MDFETs, of course, consisting of the increased dimension and the interaction of the several parameter cardinalities, carry with them a number of conceivable troubles. Some common challenges can be as listed below:

i. **Fabrication Complexity**: Manufacturing FETs with more than one gate or more than one dimension often requires state-of-the-art fabrication techniques, which are usually expensive and difficult to scale up.
ii. **Material Compatibility**: Employing different materials for different parts within the transistor, using different semiconductors for channels or gates, further introduces material compatibility problems, reducing reliability in a device.
iii. **Gate Control and Leakage**: Multiple gates demand great accuracy in control, avoiding the menace of leakage currents in order to operate the transistor properly. With increasing dimensions, this task becomes harder [40].
iv. **Dimensional Scaling**: As the dimensions continue to shrink in order to gain higher performance, it becomes hard to keep all the dimensions uniform and reliable.
v. **Signal Crosstalk**: Multi-gate FETs pose a problem in terms of isolation between different gates due to signal interference or crosstalk.
vi. **Thermal Management**: Higher packing density and increased complexity raise the resulting temperature, for which effective thermal management has to be devised.
vii. **Process Variability**: Variability in the fabrication process can lead to variations for different dimensions or gates differently, causing inconsistency in device performance. Meeting these challenges requires yet more materials science, device design, fabrication techniques, and integration process advances before the full MDFET potential can be realized for future electronic applications [41].

2.5.2 Improvements of Multi-dimensional FET

The advancement being pursued to enhance MDFETs relates to overall performance, scalability, and capability. The following are the main guidelines of advancement being pursued:

2.5.2.1 Performance Advancement

i. **Increased Speed**: MDFETs pursue expanded speeds in order that digital devices can run faster.
ii. **Decreased Power Consumption**: Advances are focused on decreasing leakage currents and enhancing efficiency, as these are both vital in low-power digital gadgets.

2.5.2.2 Dimension Scaling

i. Advances in nanofabrication strategies can lead to smaller dimensions, which may exponentially growth transistor density, and consequently, allowing growing capability on an unmarried die [42].
ii. **Improved Gate Control**: Continued improvements in gate materials and gate systems allow elevated manage over transistor motion. Needs the transverse measurement to be accurately small, and leakage to have been reduced in order that performance may be safely increased.

2.5.2.3 Material Advances

i. Continued development of the latest semiconductor materials that have better electrical residences than silicon and are compatible with new dimensions to decorate usual performance and reliability.

2.5.2.4 Functionality and Versatility

i. **Multi-gate Architectures**: Designs incorporating more than one gates permit for finer management over transistor operation, enhancing overall performance metrics like on–off ratios and switching speeds.
ii. **Integration with Other Technologies**: MDFETs may be integrated with sensors, memory factors, and different additives, permitting multifunctional and flexible device applications [43].

2.5.2.5 Reliability and Stability

i. Improvements in manufacturing techniques and substance's goal to beautify tool reliability, toughness, and stability beneath diverse running conditions.

2.5.2.6 Thermal Management

i. Techniques for green warmth dissipation and thermal control ensure strong operation even at excessive frequencies and densities.

2.5.2.7 Scalability and Manufacturing Efficiency

i. Advances in fabrication techniques, which include superior lithography and deposition techniques, improve scalability and reduce production expenses, making MDFETs handier for business applications.

2.5.2.8 Emerging Technologies

i. Exploring novel principles like quantum-dot FETs, carbon nanotube FETs, and other rising technologies could unencumber new possibilities for overall performance enhancements past traditional semiconductor procedures.

These improvements together aim to push the limits of digital tool capabilities, permitting faster, smaller, and more electricity-efficient technology for destiny packages.

2.5.3 Future Directions

The future of MDFETs may be miniaturization development, increasing electricity efficiency, new substances—2D substances and quantum dots—and integration with emerging technologies such as quantum computing and neuromorphic computing. Those physics concepts are important for the optimization of MDFET designs and the capability to exploit their potential in next-generation electronics and computing programs [44].

2.6 SUMMARY

A MDFET is a modern-day transistor that makes use of three-dimensional structures for increased performance and efficiency in comparison to traditional planar devices. The key players in this category include FinFETs, multi-bridge channel FETs (MBCFETs), and GAA FETs, all of which aim at reducing leakage currents while enhancing gate control over the channel. These transistors provide much better functioning, less power consumption as well as improved scalability for advanced semiconductor nodes because they allow the gate to control the channel from several directions at once. Therefore, with respect to conventional planar transistors reaching their limitations, such designs are necessary for sustaining Moore's Law.

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3 2D Material-Based Field Effect Transistors (FETs)

Piyali Saha, Soumya Sen, Prabhat Singh, and Ashish Raman

3.1 AN INTRODUCTION OF 2D FIELD EFFECT TRANSISTORS

In addition to providing the essential framework for the present-day information to the community, the semiconductor sector also developed cutting-edge technologies that generated $595 billion in worldwide industrial sales by 2021 [1].

Additionally, a large range of consumer gadgets that are directly tied to people's daily lives employ semiconductors extensively. The metal oxide semiconductor field effect transistor (MOSFET) layout founded on silicon has been widely used in the field of semiconductors for many years [2,3]. The recent development of nanotechnology technique has led to a continuous reduction in MOSFET substrate size. For example, a 32 GB memory stick can have over 256 billion MOSFETs, and just one chip can have more than 2 billion MOSFETs. But as MOSFET sizes continue to drop, a few problems have recently surfaced [3].

3.1.1 MOSFET STRUCTURE

The four basic MOSFET topologies that are commonly seen are the n-type boosting mode MOSFET, as detailed in Figure 3.1, the n-type depletion mode MOSFET, the p-type enhancement-type MOSFET, and the p-type depletion-type MOSFET [4]. As seen in Figure 3.1, we present a conventional n-channel enhanced-mode MOSFET here [3]. The two extensively etched n-type silicon areas of the n-channel enhanced-phase MOSFET are wherein the majority transport are electrons since there are significantly more electrons than holes in these locations. The aforementioned two places are the places where drain and source terminals are connected. A chunk of p-type silicon links these two spots. This silicon has more holes than electrons. A skinny layer of insulating material covers the p-type silicon and the gate. This stops current from leaking through the gate while the device runs. The device has grounding at both the source and p-type silicon, as well as the drain gets biased with a voltage that is positive when a positive voltage is provided. A depletion area is created when the voltage regulates the flow of electrons from n-type silicon toward p-type silicon. The two depletion zones open up with a specific applied positive voltage increase. This allows current to flow through turning on the MOSFET. However, if the voltage is too low or negative, the connection won't form. Because of this, flow of current in between the source and drain is stopped. For that case, the MOSFET is declared to be turned off. Because they exhibit on–off characteristics, MOSFETs act as switches.

DOI: 10.1201/9781003543923-3

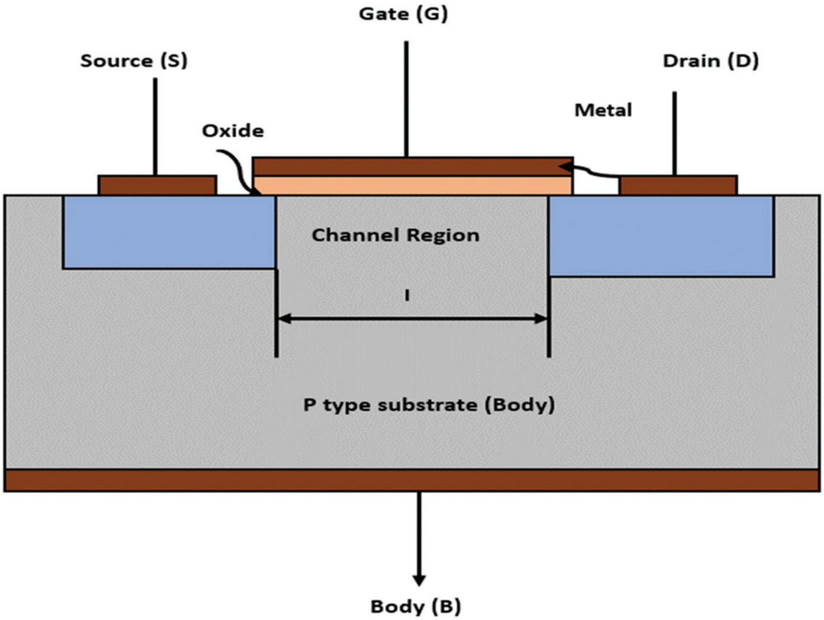


FIGURE 3.1 Typical n-channel enhancement-mode metal oxide semiconductor field effect transistor (MOSFET).

3.1.2 MOORE'S LAW

In 1965, Gordon Moore proposed the now-famous Moore's Law. It explains that a chip's transistor density will double every 2 years [5]. This rule has held true for over 50 years driving the creation of devices like smartphones and computers. To keep up with this law, engineers need to shrink transistor sizes. This allows silicon wafers of the same size to fit more transistors boosting the chip's capabilities. But Moore's Law isn't just about doubling transistor count. It also predicts a decrease in transistor costs and a boost in transistor performance. One way to achieve this is to speed up the chip's processing while cutting down on its power use. Figure 3.2 shows the Moore's Law graph up to 2030.

Currently, more than 2.5 trillion MOSFETs may be arranged on a silicon wafer [6], a doubling of the transistor count, but it also necessitates a drop in the price and enhancement in each transistor efficiency.

3.1.3 SHORT-CHANNEL EFFECT

As MOSFET sizes have been continuing to shrink over the past few years, a number of associated issues have emerged along with growing technological difficulties. The one that affects the chip's functionality the most is the short-channel effect. The MOSFET starts to show signs of rising off-state current as its channel gets shorter and shorter [3,7]. This indicates that even though the gate voltage is used to inhibit current flow, certain carriers are still able to travel freely across the drain and

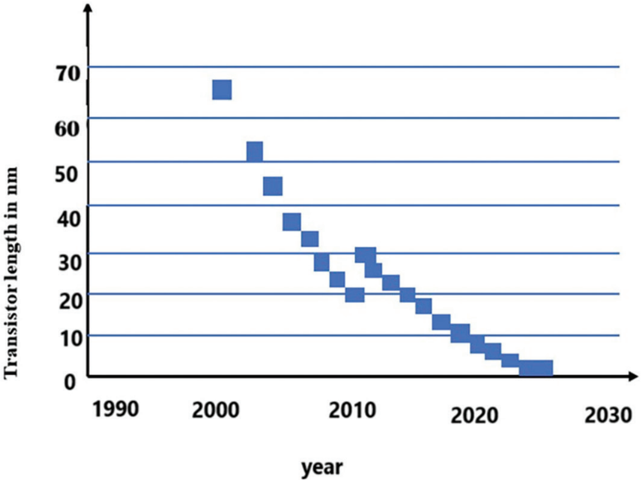


FIGURE 3.2 According to Moore's theory, as a chip's transistor count rises over time, so does the number of transistors that can be produced on it. The best-case scenario is shown in this graph until 2030.

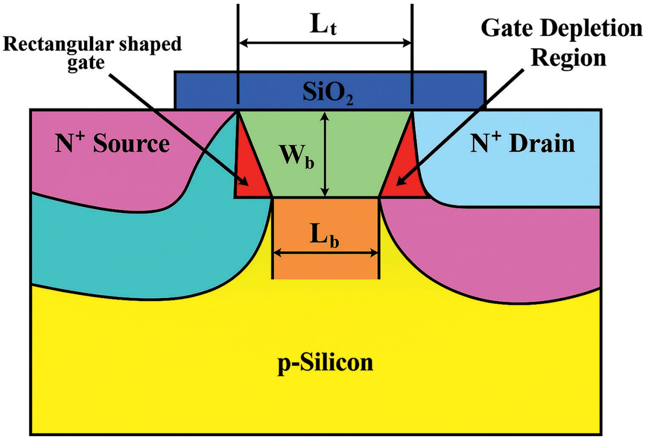


FIGURE 3.3 Short-channel effects in metal oxide semiconductor field effect transistors (MOSFETs).

source. In particular, at the time of the channel length l is scaled, the drain-end electric field channel is increased. This develops a greater possibility that an electron may tunnel through the oxide layer and thereby shorten the channel effectively. This could be harmful to transistor performance and lead to inefficiencies in energy use because such a situation enhances the threshold voltage and reduces the drain current. The typical functioning and efficiency of MOSFETs are greatly impacted by the different short-channel effect, which is shown in Figure 3.3 [1].

As a result, Moore's Law approximation has been updated by the ITRS (International Technology Roadmap) for semiconductors from twice the number of MOSFETs every 2–4 years to every 3 years. Currently, there are essentially two approaches to address the different short-channel effects. One is to alter the semiconductor material used in MOSFETs; for example, 2D materials like MoS_2, WeS_2, and BP might be used in place of silicon [8].

3.1.4 2D FIELD EFFECT TRANSISTOR

The usual method for creating ultrathin body semiconductors (a few atomic layers) from three-dimensional substances like silicon is to progressively increase the size of MOSFETs [9].

The issue with these very thin semiconductor bodies is that they still have a lot of dangling connections on their outermost layer. As the thickness of the substance decreases, these dangling bonds can significantly affect the device, and worse, propagate charged particles through ligand migration and strongly influence carrier mobility in the device (Figure 3.4a and b) [9,10].

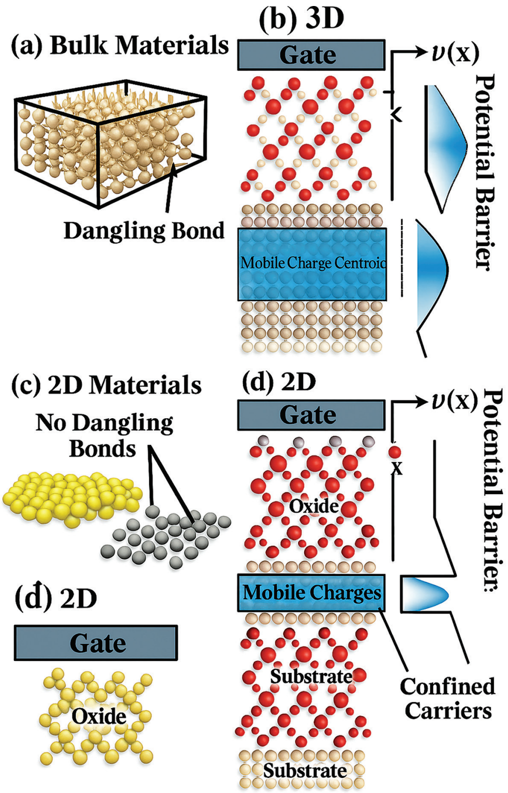

(a) Bulk Materials
Dangling Bond
(b) 3D
Gate
ν(x)
x
Potential Barrier
Mobile Charge Centroic
(c) 2D Materials
No Dangling Bonds
(d) 2D
Gate
ν(x)
x
Oxide
Mobile Charges
Substrate
Substrate
Confined Carriers
Potential Barrier
(d) 2D
Gate
Oxide

FIGURE 3.4 The benefits of 2D materials for FETs over 3D materials: (a) the electric property of field effect transistors is degraded by the dangling bonds and defect states of thin bulk, (b) electrostatic field regulated by the gate and carrier distribution of three-dimensional semiconductor material, (c) two-dimensional semiconductor material with atomically smooth surface, and (d) carriers in two-dimensional semiconductor material are confined in nanometer-scale channel and thus highlight the gating effect [2,10].

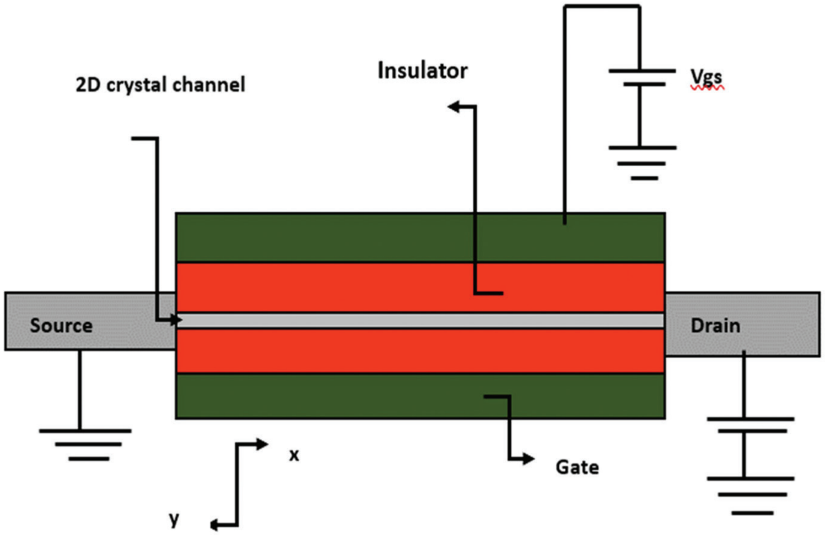


FIGURE 3.5 The 2D field effect transistor's structure. The gate voltage is V_{gs}, and the drain bias is V_{ds}.

As seen in Figure 3.4c and d, in contrary, 2D substances lack hanging bonds and fault states, which makes them extremely smooth at the quantum level [11–13]. Furthermore, 2D substances are impervious to the short-channel effects due to their tiny thickness. A 2D field effect transistor (FET) is a transistor in which a 2D material is used in place of the conventional silicon used in MOSFETs [14]. There is little structural difference between a 2D FET and a conventional MOSFET. A 2D FET's fundamental structure is depicted in Figure 3.5. According to a conventional MOSFET, a 2D FET operates on the basis that current flows across the source and drain whenever a forward voltage is provided, turning on the transistor. The transistor shuts off when the voltage being applied is insufficient or becomes negative. Furthermore, the invention of 2D FETs has a promising future thanks to the broad band gaps of 2D semiconducting substances [15–20].

3.2 WORKING PRINCIPLE OF 2D MATERIAL-BASED DEVICE

Chapter 1 introduces some basic concepts about FETs.

In essence, a FET is a device with three terminals: a source, a gate, and a drain. Complex logic circuits are based on FETs, and typical FETs are made of channel material made of big semiconductors like III-V or silicon [21]. Nevertheless, as Figure 3.6a illustrates, the channel component of 2D-layered semiconductor materials–based FETs will use 2D semiconductor materials. Figure 3.6b depicts the ball-and-stick model of the 2D semiconductor material. Usually, the substrate is highly etched silicon over which a thin layer of silicon dioxide forms. The 2D semiconductor material's ball-and-stick concept is shown in Figure 3.6. Typically, the highly etched silicon is topped with a thin layer of silicon dioxide, which serves

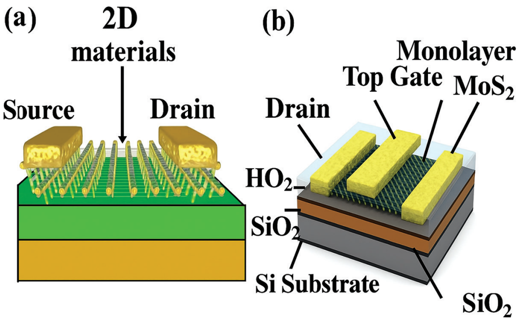


FIGURE 3.6 Diagrammatic representations of two distinct kinds of 2D stacked FETs: (a) one has the top-gate voltage applied, and (b) the other has the rear gate voltage applied [23].

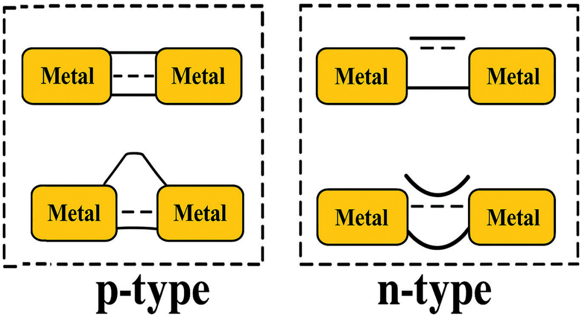


FIGURE 3.7 Diagrams illustrating the energy band structure of a p-type and an n-type field effect transistor.

as the substrate. The 2D semiconductor material's source and drain terminals have been penetrated by the metal. It is possible to apply gate voltage to the severely doped silicon [22]. It applies an electric field over the silicon dioxide insulating layer and creates an electrostatic field that can vary the amount of carriers in the channel material. As the carrier density of the channel varies, the source–drain current changes as well. Top-gate designs are frequently used in the design of FETs in order to improve gate control. The first single-layer molybdenum disulfide FET with a top-gate architecture is depicted in Figure 3.6b and was developed by A. K is [23]. Top-gate designs can more effectively address the issue of state defects in silicon dioxide because their insulating layer is usually composed of aluminum oxide and hafnium oxide as opposed to back-gate structures.

With the use of band sketches, the operation of FETs utilizing 2D semiconductor compounds is typically described and demonstrated. Figure 3.7 depicts the diagrammatic drawings for band structures of the both n-type and p-type FETs, respectively. Because of these distinctions, metals and semiconductors have different work functions that have historically been inaccessible. This difference represents the potential for interaction. The band arrangement of the semiconductor substance will be twisted after interaction because the metal and semiconductor's Fermi levels must be at the exact same point to create thermal equilibrium. This bending forms a barrier where metal and semiconductor come together. The expansion or lowering of this barrier is the principle of operation for the FETs based on 2D material. Using p-type substances as an example, holes are the primary carriers and are in charge of transmitting positive charges in these sorts of substances. P-type substances have a Fermi level that is within the band gap with their equilibrium condition. Fermi level rises in the valence band when a negative gate voltage is supplied, boosting the quantity of carriers of holes that may be conveyed freely, decreasing the contact possibility, and raising the current. In n-type substances, the opposite is true! The Fermi value of n-type substances is within the 12 bandgaps in thermal equilibrium. Under a supplied positive gate voltage, Fermi level shifts in the direction of the conduction with the increment of the concentration of electron carriers, decreases contact potential, and increases current.

3.2.1 I-V CURVE

MOSFETs possess two states, on and off. In an example of n-channel enhancement-mode MOSFETs, while the on condition implies the channel itself is in a conducting state and a large number of current flows through the channel area. By definition, the current flowing through the device in on condition is equal to: I_{ON} at $V_{GS} = V_{DS} = V_{DD}$. When the bias potential of the MOSFET is at VGS = 0 V and VDS = VDD, there's only a very tiny off-state current because the channel impedance is quite low. The voltage at which the onset of conduction starts is referred to as threshold voltage or VTh. The transfer characteristic of an n-channel enhancement-mode MOSFET is shown in Figure 3.8. The drain current Drain current (I_{DS}) gradually becomes a function of the gate–source voltage VGS in the below threshold region, where there

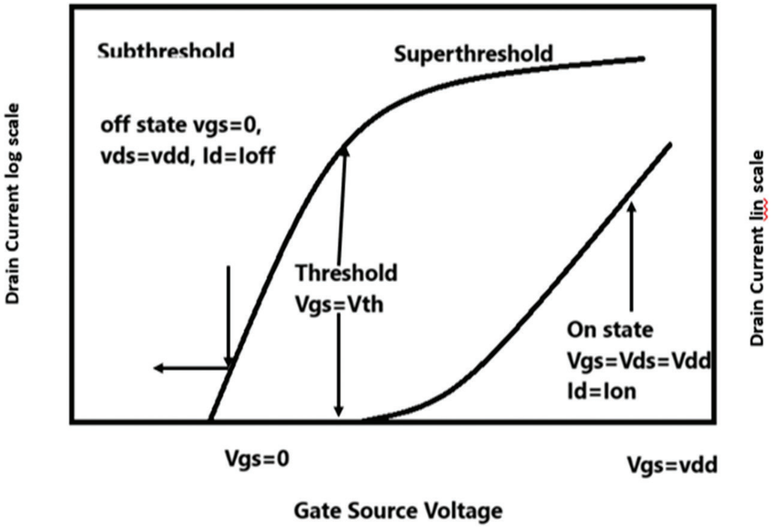


FIGURE 3.8 Transfer characteristic curve of n-channel field effect transistor.

is a crossover zone that is practically exactly at the threshold voltage. Eventually, the curve reaches the suprathreshold region, that is, when IDS and VGS become a linear function [24]. The abruption from the subthreshold to suprathreshold regions can correspond directly with the last 25 years, where the power supply voltage VDD of logic complementary metal-oxide-semiconductor (CMOS) circuits was reduced parallel to the continued decreasing dimensions of the MOSFET. As science, technology, and processing are improved and lower the MOSFET invention size, it can be seen that, moreover, the MOSFET size can still be further decreased. Put another way, the ability to regulate the on and off phases for MOSFETs along with a very modest gate voltage is currently required for the forthcoming generation of MOSFETs. The MOSFET's on/off ratio is additional crucial characteristic [25, 26]. For MOSFETs to function as required in today's digital logic circuits, their on/off ratio must be between 104 and 107 [8]. Quick on-state current as well as on/off ratio and lower off-state current are the optimum conditions since they indicate rapid switching appraise and lower static power utilization, respectively. Carrier mobility is another crucial metric for assessing MOSFET efficiency. Because of its increased carrier mobility, the MOSFET may operate at quicker speeds and use less power. The maximal transport capability of each unit MOSFET in today's silicon-based logical circuits is limited to 1000 $cm^2/V/s$, yet there is still more space for development [27]. Thus, the goal of research continues to identify substances that can substitute silicon and have high carrier mobility.

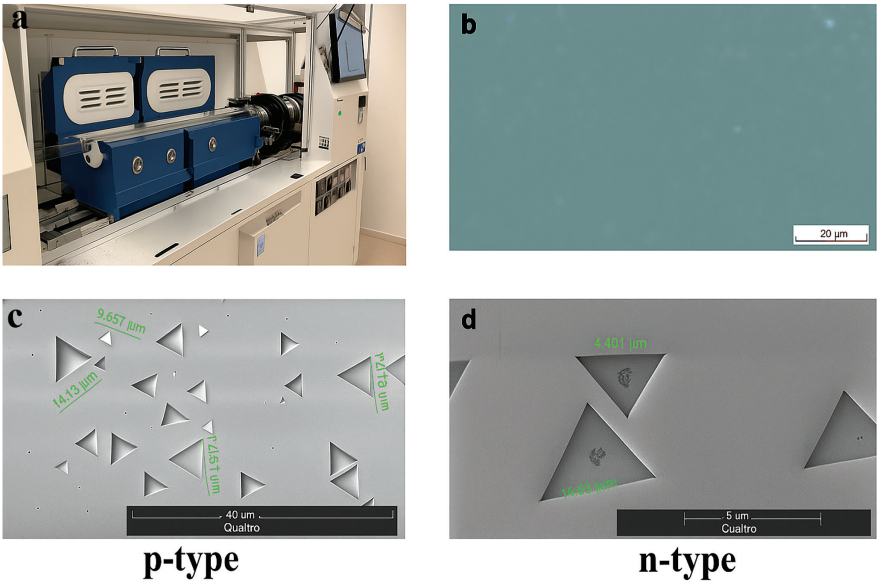
3.3 MANUFACTURING PROCESS OF 2D MATERIALS–BASED DEVICES

3.3.1 2D-Layered Materials Preparation

Many methods including liquid-stage depilation chemical vapor deposition (CVD) and mechanical exfoliation molecular mechanism epitaxy can currently be used to make a 2D layer of material.

For the purpose of generating 2D substances like graphene, 2D TMDs, and hBN, CVD is a commonly utilized technique [28–33]. A CVD apparatus, optical microscopy, and scanning electron microscope pictures of 2D WSe_2 grown via CVD are displayed in Figure 3.9 [34].

By being heated, plasma excitation, or laser radiation of gaseous and vapor-phase chemical compounds, CVD is a process that leverages chemical processes to generate solid accumulations at the gas–solid junction. In general, there are multiple phases in the CVD process, as Figure 3.10 [35] illustrates. Before the reaction begins, the impurities, oxides, and other contaminations in the surface of the substrate must be removed and treated to ensure that the surface of the substrate is both pure and smooth. After that, and controlling and scaling the gas feed rate, the reaction gas will be injected into the reaction chamber. The reaction gas can be a single gas or a combination of more than one gas. In order to provide enough energy for gas molecules to reach a point to react, the reaction gas must be heated to the proper reaction temperature. Upon entering the reaction chamber through the intake, the heated combustion gas dissipates and moves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Cualtro
p-type
n-type

FIGURE 3.9 (a) CVD apparatus, (b) 2D WSe_2 optical microscope image, and (c, d) 2D WSe_2 SEM image [34].

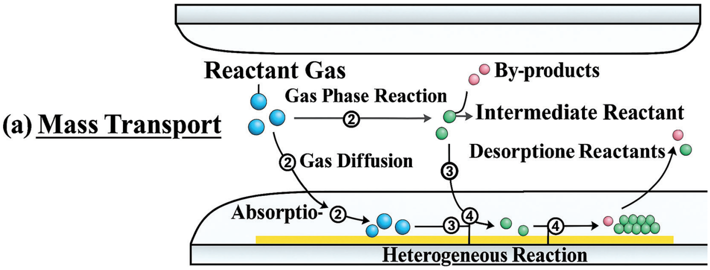
(a) Mass Transport
Reactant Gas
Gas Phase Reaction
②
By-products
Intermediate Reactant
② Gas Diffusion
③
Desorptione Reactants
Absorptio-
②
③
④
④
Heterogeneous Reaction

FIGURE 3.10 The process of obtaining two-dimensional materials by mechanical exfoliation: (a) bulk two-dimensional semiconductor materials and (b) semiconductor layers torn from two-dimensional materials after repeated folding [34].

throughout the reaction chamber through convection, diffusion, and other means. The completed reaction product will be left on the substrate surface after the gas molecules have reacted with the base surface. The feedback commodity will deposit and, with time, will make a thin film on the base surface. Once the reaction product has been deposited, the waste gas and unreacted gas can be removed from the reaction chamber. To ensure that the product and gas deposited on the substrate surface do not stay in the reaction compartment, the substrate and the reaction compartment can be cooled to terminate the reaction. CVD has advantages including the capability of materially grown large-area films, much faster than other methods of thin-film deposition, and does not require high-vacuum working conditions. CVD can generate vast quantities of single-layer or few-layer 2D semiconducting materials, but long processing times, complicated procedures, and unstable growth conditions remain issues. Furthermore, large-area transfer is challenging to do.

In order to create and build thin films alongside sizes that vary between hundreds of nanometers to microns, J. N. Coleman et al. [33] have most recently interconnected combinations of compounds in media like N-methyl-2-pyrrolidone (nmP) and N, N-dimethylformamide (DMF), followed by the implementation of ultrasonic sound or shear mixing to diminish the layer placed between other layers van der Waals dealings. Subsequently, the combinations of varying thicknesses were fast centrifuged for layer separation purposes. To create layer substances, the researchers then altered the outer tension of the mixture via surfactants or benign organic solvents (e.g., IPA). X. F. Duan et al. [24] encountered problems with manufacturing large amounts of liquid-phase exfoliated 2D materials that all had a consistent size. Notwithstanding, their liquid-phase exfoliation access produced flat conductive matter films excelling inch mobility. The measurement of 2D semiconducting films obtained from the liquid-stage depilation of 2D substances is often less than a few cm^2/V due to the presence of residual organic chemicals and severe transport dispersion during layer penetration. Before the gadget is constructed, the block material needs to be prepared. It is on to amp man of pre-cut cross record and incessantly accordion. The tape's adhesive properties cause the van der Waals attachments between the 2D semiconducting layers to break. As seen in Figure 3.11, a smaller 2D substance with less thickness can be produced with the right number of adherences. After adhering to polydimethylsiloxane (PDMS), the substance on the adhesive tape is dry transported to a fixed location on a silicon/silicon dioxide surface. Scientific study frequently uses hybrid structures and 2D stacked conductive substances that are generated by mechanical exfoliation because they can produce higher contact quality. However, it is challenging to apply this technology to industrial production since it takes a lot of time, requires some knowledge, and is tough to employ for preparing large-area materials.

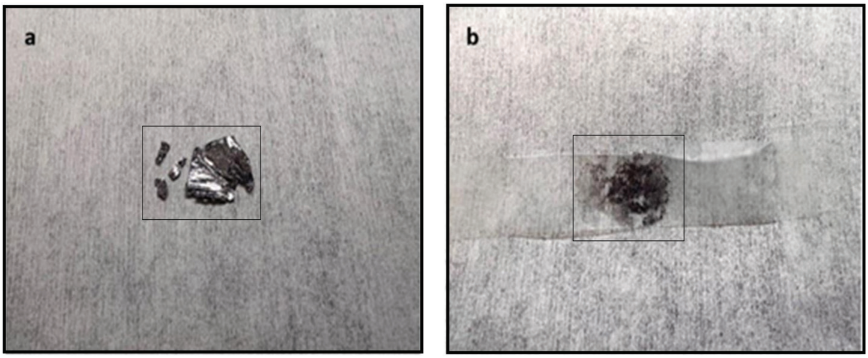

FIGURE 3.11 Diagram showing the basic general steps in a typical CVD method [35].

3.3.2 2D LAYERED MATERIALS TRANSFER

We used both wet transfer and dry transfer as 2D substance transfer techniques in this work. Whereas the 2D substance employed for dry transfer was generated by mechanical exfoliation using bulk substance, the 2D substance utilized for wet transfer was produced by CVD on a silicon dioxide/silicon platform.

Prior to the wet transfer procedure, silicon dioxide, the silicon sample, and the 2D material were all surface-coated with a layer of poly (methyl methacrylate) (PMMA). Because the 2D material to be transferred is thin, the PMMA layer functioned as the handles layer and offered capabilities to alleviate difficulties during the transfer process. After being sliced to the appropriate size, the sample was put on a surface treated with buffered oxide etchant (BOE). The silicon dioxide coating in the center of the specimen is removed utilizing BOE's oxide-etching ability, which separates the 2D substance from the silicon backing and causes it to hang on the BOE's interface. After being removed from the BOE with a glass slide, the PMMA/2D material was quickly dipped into a Petri dish of deionized water to rinse off the residual BOE. After being rinsed, the 2D material was cleaned up. The substance was subsequently carefully pulled onto a perfectly clean silicon dioxide/silicon surface and allowed to dry in an exhaust hood. PMMA was eventually eliminated from the surface of the 2D material by immersing the transferred sample in acetone. The completed copied sample is depicted in Figure 3.12 [34].

The silicon/silicon dioxide surface was placed on a three-coordinate displaced platform and put under an electron microscope during the dry transferring process. In order to approximately correlate the preferred location of the 2D substance on the PDMS with the region on the surface where the substance was to be passed on, a PDMS-coated glass slide containing the intended 2D substance was subsequently set on a fixed point on a separate three-coordinate movement platform. Figure 3.13 [34] depicts transferring a device. The experiment's particular thickness of the 2D

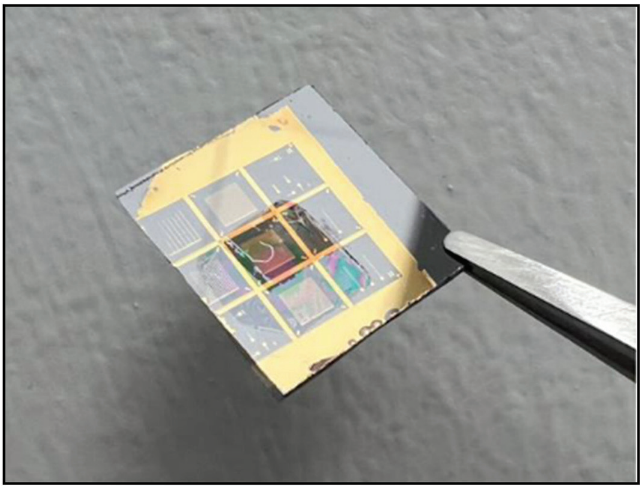

FIGURE 3.12 Wet transfer two-dimensional material to substrate [34].

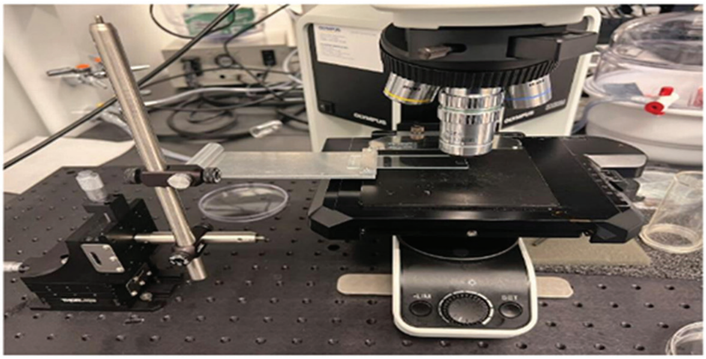

FIGURE 3.13 The dry transfer device [34].

semiconductor material was ascertained by using an optical microscope to examine the various colors. The backing material had been heated by a thermostat regulator and secured with sticky tape on the three-coordinate displaced platform throughout the transfer procedure. During the movement of thick and large-area substances, steaming was utilized to harden the PDMS, improving the material's interaction with the platform.

3.3.2.1 Substrate Preparation

In this work, silicon dioxide surface developed on highly etched p-type silicon is utilized. The silicon dioxide has a width of x nm. Markings must be applied to the substrate beforehand to make the future lithography using electron beams and other operations easier. To generate the inscriptions, the silicon wafer must first be cleaned. Soak the wafer in acetone for 20 seconds while sonicating it. Afterward, rinse the surfaces of the silicon wafers with isopropanol and deionized water. Following this, the silicon wafer is scrubbed and baked for 2 minutes at 105°C. Finally, the sample is exposed to UV lithography, applying LOR10B and S1805. The spin-coating process calls for spinning at speeds of 3000 and 2000 rpm for 1 minute, followed by baking for 10 minutes and 1 minute, respectively. To get the markings on the substrate, the substrate is next subjected to UV light for 10 seconds, and then it is developed for 70 seconds. After that, 50 nm chromium and 450 nm gold are generated at the designated places using electron beam deposition. The layer of chromium acts as a link between the higher gold layer and the 22 substrates. The photoresist is then removed using acetone during the lift-off procedure, revealing the marks.

3.3.2.2 Spin Coating

It is necessary to apply two layers of photoresist before performing electron beam lithography. The photoresist-covered portions will be exposed by the electron beam's activity during electron beam lithography. In this chapter, PMMA950 A6 and PMMA950 A2 photoresists were employed. To achieve a homogeneous distribution of the photoresist, PMMA950 A6 is first spin-coated, accelerating at 500 r/s to 800 r for 15 s. Next, the experience is to accelerate to 2000 r for 60 seconds, at an acceleration of 1000 r/s. Next, the PMMA film is warmed up at 180°C on the highly seasoned plate for 1 minute. The photoresist is then uniformly distributed by spin-coating PMMA950 A2 at an acceleration of 500 r/s up to 1000 r for 15 s. The following stage involves warming on a highly seasoned plate for 1 minute at 180°C after accelerating for 60 seconds at a rate of 1200 r/s up to 3000 r/s.

3.3.2.3 Electron Beam Lithography

This chapter uses electron beam lithographic (EBL), which is comprised of an nanometer pattern generation system (NPGS) operating system and an electron scanner. Using design CAD, the electrode is drawn on a snapshot taken at a 50× resolution under a light microscope. After that, it is transferred into the NPGS structure, where brightness and amplification settings are adjusted. The image is subsequently positioned with the real scenario utilizing a scanning electron microscope and the pre-made marks. The electrode is finally exposed to the designated spot.

3.3.2.4 Developing

For development of the areas that have been exposed, a surface containing the substance must be put in the developer mold after the exposure is finished. The substrate is first steeped in the buffer solution for 1 minute, followed by the developer, which is MIBK: IPA = 1:3. Positive photoresist means that the exposed portions will show through.

3.3.2.5 Metal Deposition

This phase can be completed using either thermal evaporation or e-beam evaporation. The substrate must first be fixed into the evaporation chamber. After the chamber has been evacuated to 10–5 Pa with a mechanical and molecular push, activate the electron cannon. The metal in the crucible will be bombarded by the electron beam, vaporizing it. Because of the lower base temperature, it will bind to the base surface when it comes into touch with it. This procedure involves depositing 350 nm of gold after depositing 5 nm of titanium. The gold nanoparticles utilized in this chapter are 99.99% pure gold. To determine the material's depth on a wafer of silicon, utilize a depth gauge. The coating process is finished when the required thickness is attained.

Note that only when the thickness is greater than 6 nm will the metal create a homogeneous coating. As a result, in order to raise the electrode's excellence, the rate of deposition must be tightly controlled initially.

3.3.2.6 Lift-Off

The lift-off method utilizes photosensitivity to disintegrate in acetone to break down the photoresist itself. This allows the metallic material on top to fall off as well, leaving just the metal at the 24 electrodes. Isopropanol is then used to get the surface cleaned. Hence, the production of the electrodes of the gadget is completed. The image in Figure 3.14 visualizes the whole process.

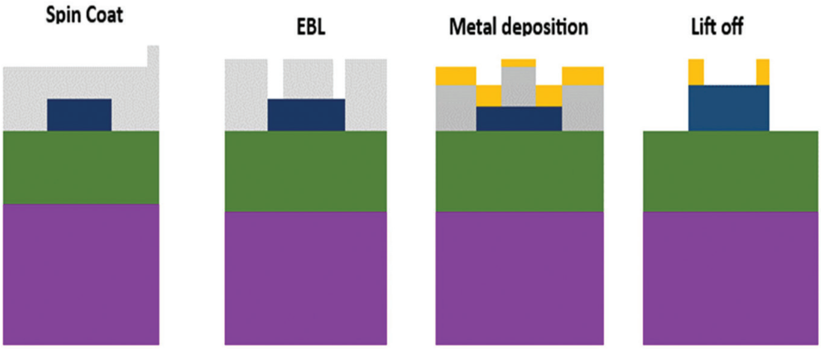

FIGURE 3.14 Electrode fabrication process of the device.

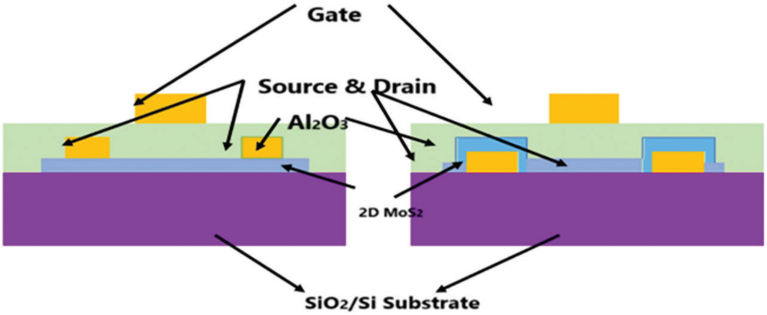

FIGURE 3.15 Diagrammatic representation of the devices in (a) the first sequence and (b) the second sequence.

3.4 2D FET

To make 2D FET devices using the methods described earlier, we create 2D FET devices in this chapter and evaluate their electrical performance. The Raman spectrum of the MoS_2 2D material that was used in the devices was also examined. Finally, we analyzed how different metal-semiconductor contacts influence the devices' electrical performance.

3.4.1 DEVICE STRUCTURE

Two different production methods are used in the process of creating FET devices. The 2D MoS_2 was first transferred upon a silicon dioxide/silicon substrate, after which the drain and source charges were fabricated at top of the MoS_2, an alumina layer was grown to act as an insulator, and lastly, the gate electrode was fabricated. Initially, both the drain and source electrodes were designated on the silicon dioxide/silicon substrate, followed by the MoS_2 deposition onto the electrodes, the growth of an alumina layer, and the fabrication of the gate electrode. Figure 3.15 displays the schematic designs of the devices made with these two processes.

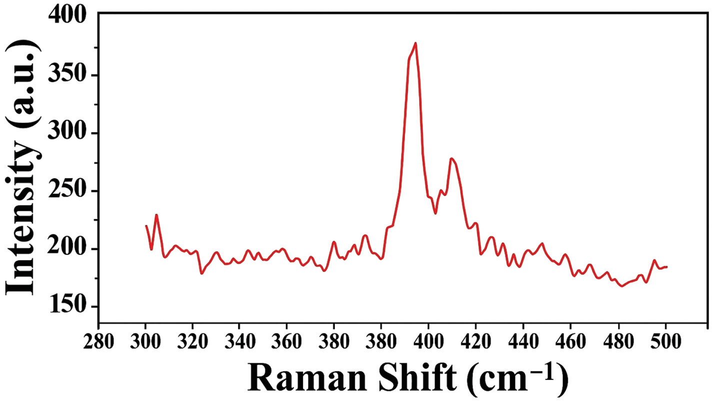

FIGURE 3.16 Raman spectrum of 2D MoS$_2$ [36,37].

3.4.2 MoS$_2$ Characterization

We took Raman spectra of MoS$_2$ using a Raman spectrum, after the sample was transferred to the base. From Figure 3.16, we see the outcome of the survey. The Raman spectrum of the material is depicted in the graph as a function of frequency, which is consistent with other previous works [36,37].

3.4.3 Electrical Performance Testing

Following device fabrication, we examined the devices' individual output curves as well as the transfer curves for the top and back gates. In Figure 3.17, the examination results are displayed. Figure 3.17a displays the output characteristic contours of the devices at different back-gate voltages. The result graphs represent the output feature of the equipment, which may be affected by varying gate voltage such as the drain–source current. The offbeat plot line reflects that the primary junction between the two materials is still a weak Schottky barrier. In addition, the work function of gold is around 5.1 eV, while that of MoS$_2$ is 4.47 eV [38,39]. Figure 3.17b suggests that by 27 the two-by-two resistance created forms a Schottky point, which is in line with the experiment results. The mentioned fault may occur as a result of the fact that the MoS$_2$ film being quite thick (Figure 3.17c displays the equipment's back-gated transfer curve using gate voltages of 0.5 and 0.2 V for the source–drain voltages). The possibility for it to occur without accurate orientation is highlighted. Figure 3.17d shows the device's top-gate transmission curves, with source–drain voltages of 1 and 0.5 V, respectively. The figure exemplifies that the device's on/off ratio is approximately 108. The device's carrier mobility can be estimated to be approximately 29.8 cm^2/V/s.

3.4.4 Metal-Semiconductor Contact's Effect on Device Performance

A contact connection is made when metallic electrodes come into contact with various semiconductor types. This port is relevant to the operation of electronic

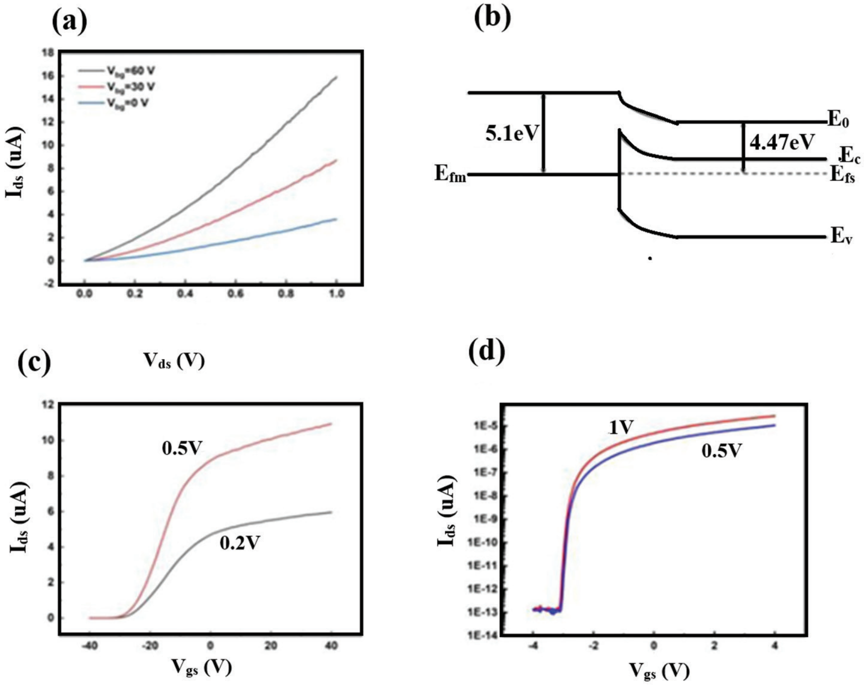

FIGURE 3.17 (a) The device's resultant curves at various back-gate voltages, (b) the Schottky contact for Au and MoS_2, (c) the rear gate's transfer curve at various source–drain voltages, and (d) the top gate's transfer curve at various source–drain voltages [34].

circuits [40]. The transmission barrier, also known as the Schottky barrier, forms at the metal–semiconductor interface. Its height, ΦBn, defines the energy needed for the carriers of charge to flow over the barrier, hence affecting the effectiveness of the charge transfer and the functioning of the device. Equation (3.1) shows how the Schottky–Mott rule can be used to predict the height of the Schottky barrier under ideal conditions [41–43]:

$$\Phi Bn = \Phi M - XS \tag{3.1}$$

Among these, ΔS represents the semiconductor's electron affinity, and ΦM represents the metal's work function. Prior to their interaction, these values are inherent characteristics of the metal and semiconductor.

However, in practical situations, the estimated ΦBn value is often much larger than the real one. Initially, interface trap states within the bandgap created by dangling bonds on the material's surface will lead to Fermi-level pinning. As a result, changes in the metal work function will make the height of the Schottky barrier more susceptible [44]. Next, to create metal using the initial fabrication sequence described in (3.1), it will be necessary to have substantial local heating to the contact region and atom or cluster bombardment. This may damage the lattice at or around the interface and thus cause defects. The phenomenon of Fermi-level pinning can also result from the gap states induced by these defects [45–47]. Thirdly, 29 chemical linkages involving the metal and semiconductor substances may emerge throughout the metal growth process. The lattice will experience strain as a result of these chemical connections, altering the barrier height and band structure [48–50]. Figure 3.18 provides illustrations of these events [51].

Yet, the foregoing occurrences can be significantly reduced by employing the second manufacturing method that is discussed in 4.1. A van der Waals contact is made when 2D semiconductor substance is transferred to metal electrodes; this prevents the emergence of gap states, the development of chemical bonds, and various other events. Figure 3.19 depicts this van der Waals metal-semiconductor connection [51].

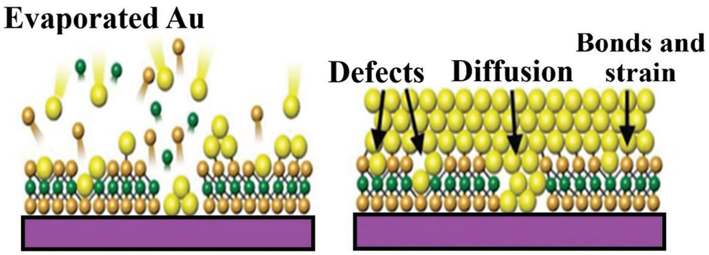

FIGURE 3.18 Defects, diffusion and bonds, and strain happen when deposit Au [51].

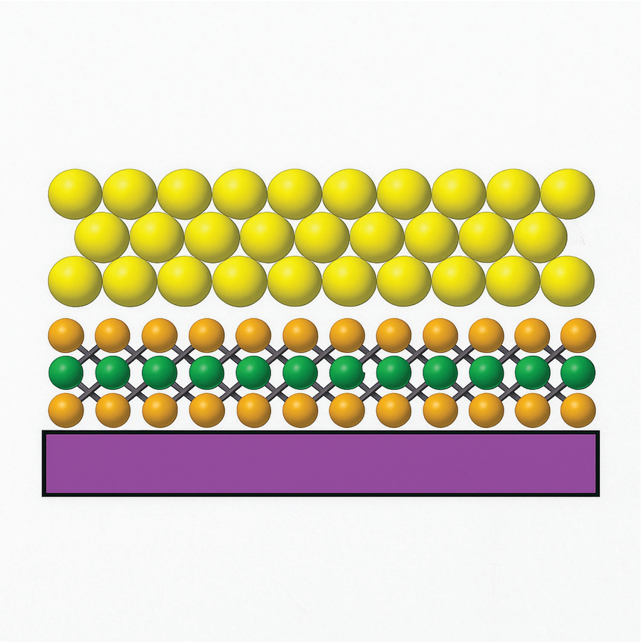

FIGURE 3.19 Van der Waals contact between Au and MoS_2 [51].

We examined the transfer profiles of the two design top gates using two distinct manufacturing patterns, as Figure 3.20 illustrates. In the test, the source–drain value of both devices was 1 V. The figure shows that the on/off proportion and carrier portability of the gadget after making a van der Waals connection are not much enhanced as we had predicted, and that the transfer profiles of the two gadgets utilizing various fabrication processes are essentially the same. One possible reason for this is that the MoS_2 we selected is not the best suitable monolayer or bilayer as it is

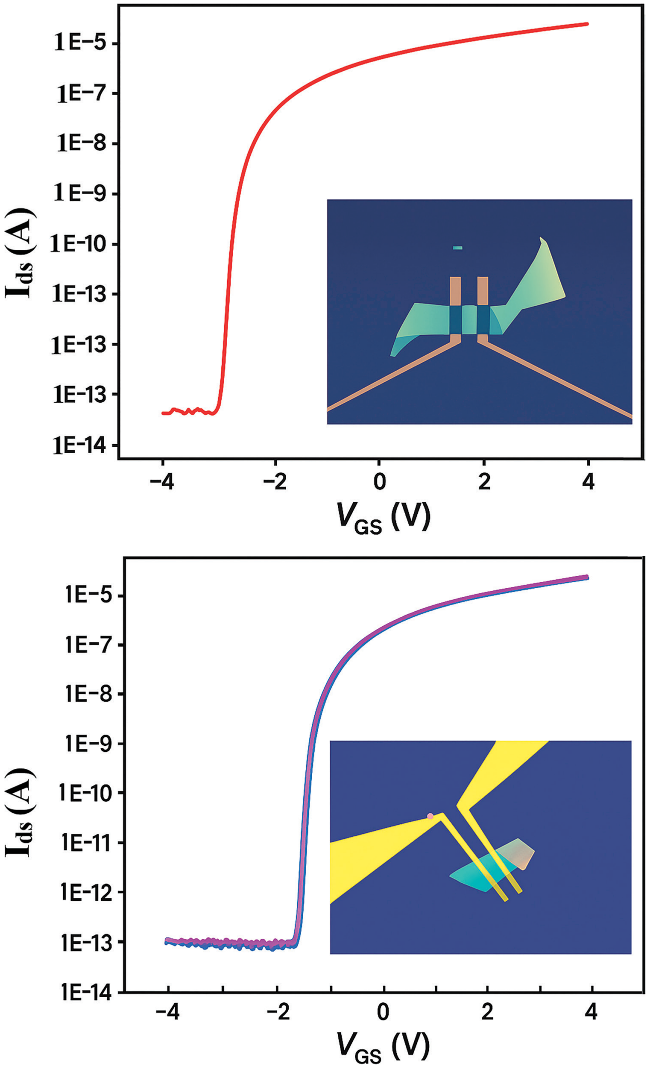

FIGURE 3.20 (a) Transfer curve of device that deposits Au first and then transfers MoS_2 (van der Waals contact), and (b) transfer curve of device that transfers MoS_2 first, then deposits Au [34].

too thick. Therefore, during the laying of Au, even if the first manufacturing process is followed, Au atoms will not go through MoS_2, thus preventing the aforementioned diffusion scenario from happening. The influence of surface-induced bond creation on the mobility of internal charge carriers gets smaller as the thickness increases.

3.5 CONCLUSION AND FUTURE WORK

3.5.1 Conclusion

The physical limit of the channel width for traditional silicon-based circuits that integrate is getting closer to the physical limit of the circuit size, and this is being achieved through continuous efforts to miniaturize them. On the other hand, the scientific community has been more interested in 2D materials due to their unique properties as materials and the enormous potential they hold for the creation of integrated electrical and optoelectronic devices [52–57]. 2D materials can be separated into different types such as p-type materials such as BP, n-type materials such as MoS_2, and bipolar materials typified by WSe_2. The FET made from gate all around (GAA) and the 2D MoS_2 FET were the main topics of this study; we covered the following:

We grasped the systematic frame constraint that chips have faced recently and illustrated the significance and the scientific background of the topic through voluminous survey resources. Then, we saw two alterations to the device's structure to turn down short-channel effect. In order to understand the potential applications of the 2D compounds employed in the research, we have finally displayed some of its fundamental physical and chemical features.

We discussed the fundamentals of FET functioning, the current–voltage curve, and a few crucial transistor performance characteristics. We presented several techniques to acquire and transport 2D semiconductor substances. Next, we covered the entire fabrication process for FET devices, the tools needed, and the tools required for growing oxide layers.

First, we designed and built a 2D MoS_2 FET, and then we performed examinations, which used the electrical characteristics and Raman spectrum of the material to deduce back-gate output profile of the mechanism and its back-gate and top-gate transference curves. Next, the impact of various metal-semiconductor contacts on the device's functionality was examined; in theory, the device with the van der Waals junction should have more than a 100% increase in efficiency under the ideal conditions. Testing was carried out to find out whether the electrical functionality gadgets made in two different orders have any significant difference. The results were most likely caused by the MoS_2's excessive thickness. We designed 2D MoS_2 GAA FET (dual-gate FET) to successively increase efficiency in 2D FET. During the manufacturing procedure, we investigated several techniques for transferring oxide layers with the goal to investigate ways to enhance the uniformity of oxide layer synthesis. Despite the possibility of a comparatively flat film with a handling layer (PDMS) approach, the device's functionality will be impacted by the difficult-to-remove etching remnant. Furthermore, there is a need to enhance this method's transmission efficiency rate. The residue in etching is solved by the alternative approach, which does not utilize a handle layer, but the transferred film is prone to creases and breaks easily. Consequently, more research into the process of transferring oxide layers is required, as is the fabrication of whole devices for the purpose of testing and comparing their electrical performance with that of 2D FET.

3.5.2 FUTURE WORK

These nanostructures as well as heterogeneous structures based on these 2D types of semiconductors can be the main objects of further research and development in light of the experimental results that are presented in this chapter. The next two directions can be used to broadly categorize future research.

3.5.2.1 Three-dimensional Logic Circuits Based on 2D Semiconductors

Electronic elements that utilize CMOS technology will need to significantly increase their efficiency in order to handle upcoming applications that require large amounts of data. These applications won't be attainable by enhancing the efficiency of individual transistors alone. Therefore, the new path emphasizes novel substances and designs for flexible and kinematically polymeric microstructures [58,59]. A 3D integrated circuit configuration is possible using this technique, which involves stacking up different semiconductor thin-film materials, unlike the existing ICs that rely on conventional planar complementing MOSFETs. Data or logical approach can be represented vertically with this structure. The new microsystem model illustrated in Figure 3.21 is capable of performing logical processes and constructing a 3D integrated circuit architecture by using various new technologies [60]. The following nanotechnology systems consist of access-memory circuits, resistive random ambient memory arrays, computer units utilizing silicon-based and carbon nanotube field-effect transistors (CNFETs), and more than 100,000 gas sensors based on inputs and based on CNP. Vertical semiconductor materials are processed to fabricate each of

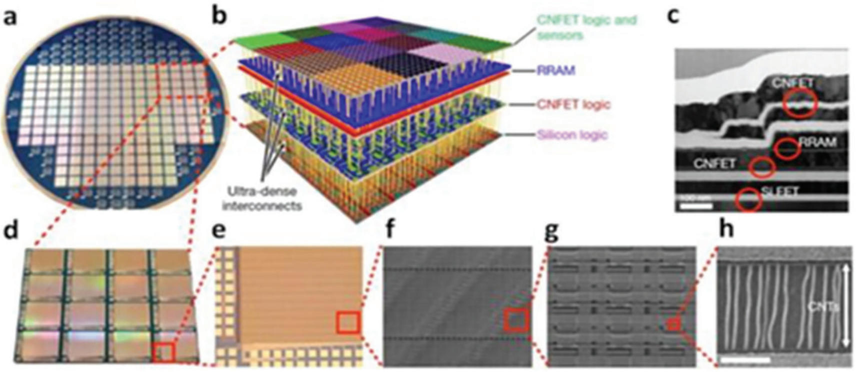

FIGURE 3.21 (a) An integrated circuit wafer measuring 100 mm in width; each unit is denoted by a red dotted line, (b) schematic diagram of the three-dimensional microsystem structure, (c) transmission electron microscopy (TEM) image of the chip, with the intervals of each layer highlighted in red, and (d–h) schematic diagram of a progressively scaled-up 3D nanosystem [60].

these sensors. The main advantages of this 3D nanosystem over the current planar nanostructure are as follows: (1) data storage using CNFETs rather than silicon transistors; (2) access-memory controls—non-volatile resistive random as opposed to dynamic random-access memory along with free exterior storage; and (3) to achieve 3D integration of all functional devices on a single silicon wafer. Atomic-layer 2D substances are also the building blocks of future 3D interconnected electronics, having been inspired by multifaceted CNFETs. 2D semiconductor substances can be utilized as dielectric layers, electrodes, and semiconductor channel materials. Graphene, hexagonal boron nitride, black phosphorus, and TMDs are a few examples of these materials.

Thus, based on 2D materials, 3D logic circuits will be a popular direction in the future [61–64].

3.5.2.2 Two-dimensional Electronic Components Based on Flexible Substrates

2D semiconductor substances have superior mechanical, electrical, and chemical characteristics that make them suitable for application on flexible substrates. Of the ones more relevant, single-layer 2D materials allow for the design of transparent electrical devices, and for this kind of materials to be fully transparent, they are only one layer thick and form 2D layers. Owing to their high Young's modulus, 2D materials might effectively bend with tolerable deflection and similar loss of performance. Compared to the traditional detectors, heterojunction photodetectors or 40 photodetectors on flexible substrates can offer a broader field of view, which means the possibility of further development of the future low-weight, large-area photo detecting and other optoelectronics [65–67].

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4 Emerging Transition Metal Dichalcogenides (TMDCs) in Semiconductor Design

A Path to Next-Generation Electronics

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4.1 INTRODUCTION

The requirement for more chip computer density has increased dramatically with the rapid evolution of technologies like autonomous driving, augmented reality, and artificial intelligence [1]. The scalability of field-effect transistors (FETs) and the integration of more transistors per unit space have allowed for this improvement in computing density in recent years. But by 2031, short-channel effects (SCEs) are predicted to cause scaling constraints for silicon-based FETs beyond the 1 nm technology node [2–4]. Considerable effort has been committed for investigating novel materials beyond silicon technology to sustain Moore's Law and for improved device designs. The surface roughness and electrostatic characteristics of silicon-based materials deteriorate when channels are narrower than 5 nm, which restricts gate length scaling below 12 nm and lowers supply voltage to less than 0.6 V [5,6]. On the other hand, atomically smooth and clean surfaces are provided by two-dimensional (2D) materials, especially transition metal dichalcogenides (TMDCs), which enhances their resistance to SCEs and positions them as promising options for post-silicon technology [7].

Gordon Moore, in 1965, anticipated that the number of components on each integrated circuit, while minimizing the cost/component, would double every 2 years [8,9]. This principle has remained effective for an additional 50 years. Moore's passing raises an enduring question regarding the future of his law: will it persist, and if so, for how much longer? Past efforts to uphold Moore's Law have mainly engrossed on shrinking transistor sizes. However, since the early 2000s, continuing to downsize transistors

DOI: 10.1201/9781003543923-4

at an exponential rate has become increasingly challenging. Moreover, as transistors have reached very small dimensions, further miniaturization leads to significant SCEs and heat dissipation that negatively impact the performance of device. Consequently, the focus has shifted toward functional scaling techniques, including strained silicon, high-k materials, metal gates, Fin-FETs (FinFETs), gate-all-around FETs (GAAFETs), and complementary FETs (CFETs) [10–13]. These innovations have allowed for "More Moore" advancements, even as the pace of dimensional scaling has slowed. Nevertheless, the continuation of More Moore is limited without transformative breakthroughs, as we are approaching to fundamental barrier. To accommodate increasingly smaller transistor footprints, the channel material thickness must be reduced in line with the length of channel for effective gate controllability. This demand creates a tailback for "More Moore" advancements, as the properties of traditional channel materials like silicon, III–V and strained SiGe compounds can vary significantly with thickness because of quantum confinement, resulting in poor device variability. Moreover, though these materials can be engineered to be atomically smooth and uniform, surface states may still reduce the mobility of thin channels. As a result, significant breakthroughs are urgently needed to overcome these obstacles.

4.1.1 OVERVIEW OF TRANSITION METAL DICHALCOGENIDES (TMDC) MATERIALS

Transition metals and chalcogens combine to form a family of materials known as TMDCs. Transition metals consist of subgroup elements (e.g., Pt, Ti, Zr, V, Mo, Nb, Ta, Hf, and W) from the element of group IIIB to group VIIIB of periodic table, and Se or S from group VIA in 1:2 ratio [14]. Because of their distinct electrical, optical, and catalytic characteristics, TMDCs have garnered a lot of interest. Nevertheless, the low conductivity of 2D TMDCs severely limits their ability to function electrochemically. TMDCs are commonly expressed as X-M-X, in which two chalcogen atoms (Se, S, and Te) in hexagonal planes covalently encircle a transition metal atom (W, Re, Mo, etc.). A family of well-characterized structures and chemistry is formed by these MX_2 compounds. Strong and persistent chemical bonds occur inside each layer; however, the bonds between neighboring layers are astonishingly weak [14]. Because of their easy simple cleavage, lubricity, and noticeable anisotropy, the crystals have drawn a lot of attention from scientists. On the other hand, their electrical characteristics are diverse. There are real metals like NbS_2 and VSe_2, semi-metals like TeS_2 and WTe_2, semiconductors like MoS_2, and insulators like HfS_2. The real metallic ones, such as VSe_2, exhibit anti-ferromagnetism band below around 150 K. All NbX_2 and TaX_2 are superconductors [15]. Metallic conductivity is provided to the compound by the partially filled outer D-orbitals of TMDC 2D materials, whereas semiconducting characteristics are obtained from fully occupied D-orbitals. The lack of dangling bonds gives TMDC materials more stability in the surrounding environment since their outer surface is filled by lone pairs containing chalcogen atoms. Because of MoS_2's resilience, it is the most researched material in the TMDC family. Intriguing prospects for basic research, MoS_2 possesses a direct controllable bandgap, strong spin–orbit coupling, atomic-scale thickness, and mechanical and electrical features. However, given the wide range of preparation procedures including chemical exfoliation, chemical vapor deposition (CVD), printing techniques, and the quick advancements in large-scale preparation technologies, 2D TMDC materials have tremendous promise for a variety of applications. To alter the electrical band structures of the materials, it is therefore usual practice to create heterostructures of materials made up of various 2D TMDCs stacked in in-plane direction (lateral structure) or out-of-plane direction (vertical heterostructure). Semiconducting TMDCs show promise in optoelectronics and photonics applications due to their bandgaps spanning from the near-infrared to the visible range [16–18]. However, in the out-of-plane direction, because of the quantum confined effect, the electrical characteristics of 2D TMDCs are significantly tuned in comparison to bulk TMDCs [19]. These materials have a strong polar surface, high surface area, high conductivity, exceptional flexibility, and a tendency to accept different cations. The ions may diffuse quickly via the MX_2 layer's interlayer gap because of the weak van der Waals (vdW) force. The MX_2 high interlayer spacing allows for the accommodation of multivalent ions including Zn^{2+}, Mg^{2+}, Al^{3+}, and Ca^{2+}. TMDCs have a limited number of active sites that are positioned on the margins, which severely limits the catalytic efficacy. They also suffer from substantial volume fluctuations during cycling, poor cycling stability, and inherently low electrical conductivity [20]. These fascinating characteristics have potential applications in the fields of pharmaceuticals, nanomedicine, DNA sequencing, personalized medicine, optoelectronics, high-end electronics, and spintronics. The optical and electrical characteristics of TMDCs, together with their applications in optoelectronics and photonics, have been examined in a few recent studies; however, a thorough examination of their biological applications has not yet been conducted. This study primarily focuses on the crystal structure, interesting features and diverse synthesis techniques of TMDCs. It also discusses how these materials are used in a variety of sectors, including energy storage, optoelectronics, electronics, biomedical, light emission, and bioimaging applications.

4.2 STRUCTURAL DESCRIPTION OF 2D TMDCs

Structurally, 2D TMDCs have resemblance with structures of graphite where each individual layer has a thickness from 0.6 to 0.7 nm [21]. TMDCs have basic chemical formula of MX_2, where M is the transition metal and the X is the chalcogen material from the periodic table. Unlike the structure of graphite that contains carbon atoms in hexagonal structures connected to other three chalcogens, TMDCs are X-M-X type three-layered sheet structure. In these layers, molybdenum is bonded with chalcogens inside the layers, and there exist weak vdW forces between the two layers. These vdW forces can be easily overcome by applying shear stress, building the lubricating properties within the TMDCs [22]. Depending on how atoms are arranged in the layers and how the layers are ordered in stack, TMDCs form either tetragonal-1T (called as octahedral) or hexagonal-2H (called as trigonal prismatic). These two phases only are thermodynamically stable phases of the material and rest all other phases formed are obtained as metastable phases. In trigonal prismatic phase, hexagonal symmetry is seen from top view, and each single layer is stacked as X-M-X in which TM atoms form covalent bonds with six neighboring X atoms [22,23]. In tetragonal-1T phase, the X atom bonds in a trigonal antiprism and trigonal fashion, respectively, in the both top and bottom SLs. This results in hexagonal top view of the atoms.

4.3 PROPERTIES OF TMDC MATERIALS

4.3.1 Electronic Properties

The electronic properties of TMDC have wide range extension from semiconductors to superconductor based on their chemical compositions. The bandgap of these materials lies in large solar spectrum from visible to infrared range. When the bulk structures of TMDCs get sliced into monolayers, the material property gets changed from indirect bandgap to direct bandgap. The reason for this change from indirect bandgap to direct bandgap can be attributed to quantum mechanical confinement of the constituent atoms [24,25]. Further, the applications of 2D materials are primarily decided by the bandgap of the material, altering the bandgap may have wide diversification in the applications. To change the bandgap of these materials, we can change the thickness of the layer, do some mechanical changes in the structure, and go for doping some new atoms in the layered structure. Also doing the defect engineering may help in altering the bandgap and, hence, the electronic properties of the material.

4.3.2 Optical Properties

For any material, the optical properties are primarily governed by its band structure. As we discussed in the previous section that the layered structures of TMDC have direct band gap structure and the band gap lying in visible range, these materials are heavily used in fabricating various optical components as well as in optoelectronic devices [26]. Optical responses in 2D TMDCs predominantly occur due to the excitons. These excitons are produced due to high Columbic force of attraction between two charge carriers, particularly electrons and holes.

4.3.3 Mechanical Properties

Defects in crystals and the method of synthesis highly contribute to deciding the mechanical properties of TMDCs. Very likely to graphene, these materials are highly strong and flexible in terms of their mechanical attributes. High covalent bonds between atoms in single layers contribute to this high mechanical strength of the materials [27].

To measure the various mechanical properties, it is very herculean task, using already existing methods used in 3D materials. But atomic force microscope is widely used to calculate mechanical properties such as Young's modulus, strain and similar other, of these materials. Mechanical flexibility of TMDCs makes them very prominent materials to be used in optoelectronic devices [28,29].

4.4 SYNTHESIS OF TMDC MATERIALS

Properties of TMDCs, be it mechanical, electronic, optical, or any other, have wide divergence depending upon its synthesis methodology. Also, the synthesized transition metal dichalcogenides (TMDs) have different applications when prepared with different method. In a broader sense, the methods for TMDCs synthesis can

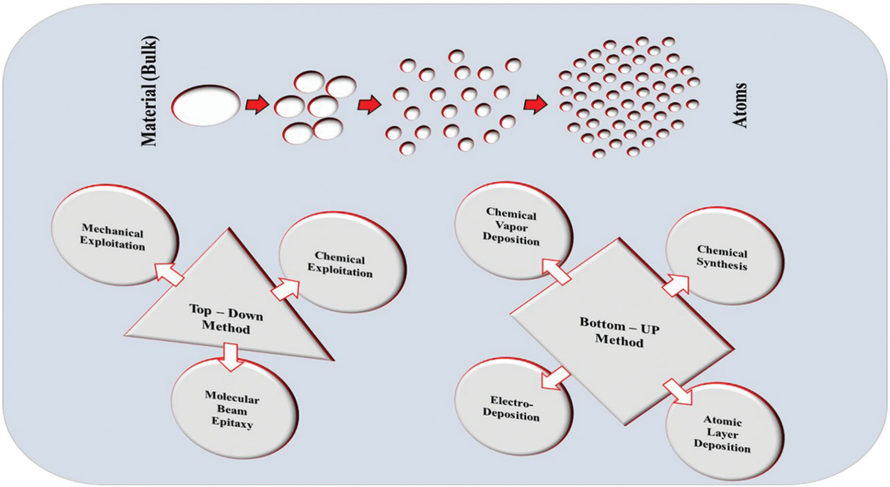

FIGURE 4.1 Synthesis techniques of TMDC materials.

be classified as methods with top-down approach and methods with bottom-up approaches. The two approaches differ in a way that whether we are starting with atoms and then depositing the layers on one substrate to form the layered material and calling it bottom-up approach or exfoliating the bulk into thin layers to form the 2D thin TMDCs as being the top-bottom approach [30,31]. The two approaches can be pictorially represented in Figure 4.1. There lie numerous positive attributes to both the approaches with fewer limitations as well.

4.4.1 METHODS FOLLOWING TOP-DOWN SYNTHESIS APPROACH

4.4.1.1 Mechanical Exfoliation (ME)

Promising applications of 2D TMDCs such as in opto-electro-mechanical devices comes from the scope to be fabricated on substrate in a single layer. Mechanical exfoliation is one such method to fabricate single-layer structures in low-dimensional materials from the bulk materials. Initially, graphene was exfoliated mechanically and fabricated on bulk with few layers. Finding the method promising, further TMDCs have also been tried being mechanically exfoliated. In general, TMDCs like MoS_2 WS_2 have been fabricated on Si\SiO_2 substrate using this method. In this method, a force is applied to peel the single layer of few atoms thickness using a scotch material tape, with such peeling sheets are cleaved from the surface forming the required single layered sheets. Layers are cleaved because the force of adhesion between the scorching tape and the material surface is quite high when compared with the van der Waals forces that exist between two atomic layers. The same process of exfoliation is carried out on the bulk material to finally find the required nanosheets [31]. However, this method of mechanical exfoliation is not preferred when catering for massive production of nanosheets as the method synthesizes poor-quality product. Also, the method does not provide dimensional control on the flakes obtained by exfoliation.

4.4.1.2 Chemical Exfoliation (CE)

The process of chemical exfoliation of TMDCs is widely done in following steps:

1. dispersing TMDC forming material in the liquid form,
2. exfoliating the upper layer of TMDC bulk material using the process of high-frequency sonication, and
3. then finally, purifying the final product obtained.

The advantage of using CE can overcome the low production yield in the case of ME. Here the successful exfoliation in achieved by inserting the catalyst material like intercalators inside the two linked layers of forming bulk material, using ultrasonication [32].

Intercalators used in the process are basically organometallic compounds. In the literature, for the exfoliation of MoS_2 into monolayers, lithium was used as the intercalor followed with the water reaction. Also, electrochemical lithiation discharge process has been utilized in the past to mass-produce highly efficient nanosheets by utilizing ethanol to produce nanolayer yield. The sonification process used here somehow increased the defects in the structure of 2D, thereby reducing the flake size. This eventually limits the application of such 2D sheets in high performance–based integrated circuit (IC) and devices.

4.4.1.3 Molecular Beam Epitaxy (MBE)

Using molecular beam epitaxy (MBE) method for synthesizing the 2D materials has evolved as proven outstanding method in the last few years [33]. MBE is a method for synthesizing thin film consisting of single crystals, and the process is performed in a condition of high vacuum. Also, the rate at which the films are grown, in MBE method, is very low to support epitaxial growth of the film. MBE provides greater control on composition and thickness of the deposited layer. Also, the different phases that synthesize in the process can also be controlled using MBE. In the last two decades, MBE method has been extensively used in producing epitaxial TMDC films [34].

4.4.2 METHODS FOLLOWING BOTTOM-UP SYNTHESIS APPROACH

4.4.2.1 Chemical Vapor Deposition (CVD)

CVD is a process driven to form thin-layer deposition on a given substrate conducted at a very high temperature. The layers are deposited because of series of various chemical reactions. The layers deposited at the substrate from this process are of high purity. The layers deposited are of atomic levels [35]. This method gets complete in two steps. In the first step, the material in gas form is sent in chamber for the reaction, and then in the second step, nanomaterial gets deposited on the substrate. The temperature inside the chamber, the time up to which the reaction continues determines the purity and evenness of layer deposited. With this method, the morphology and crystallinity along with the defects are very much controlled in the thin film deposited [36].

In the synthesis process of TMDC, the reaction precursor supplied in the chamber provides the required chalcogen atoms and transition metals (TMs). After reaction, product deposition on substrate material is atomically thin layers MX_2 (where, W, M = Mo, and X = Se, S, Te). With CVD process, even the modification required in the material properties, like tuning the band gap, mechanical and electronic properties of the 2D TMDs can be obtained.

4.4.2.2 Atomic-Layer Deposition

Owing to huge technological potential contained in TMDCs, it is need of the hour to deposit uniform films of controlled thickness particularly an ultrathin film below 10 nm. Also, the repeatability of the synthesized mono layer to form few layers thick TMDC is also very much required. Atomic-layer deposition is one such method that can build such required 2D layers in which thin film of material in gaseous phase is deposited on the substrate. The 2D TMDC obtained from atomic layer deposition (ALD) process finds its vast application in optoelectronic devices, solar cells, and in energy storage. Also, the layer-by-layer deposited WS_2 films are utilized in FETs [37].

4.5 TMDCs IN FETs

Two-dimensional (2D) crystalline semiconductors are currently under intensive investigation as potential channel materials for FETs. These 2D transistors offer several advantages, including outstanding electrostatic gate control owing to their higher surface-to-volume ratio, enhanced conductivity, and pristine surfaces, which guarantee the high interface quality with insulators [14]. Furthermore, the customizable electrical characteristics of their stacking and layer dependence offer further design options for transistors. These exclusive characteristics create opportunities to integrate 2D materials into various FETs designs, allowing for the better electrostatic control and tunneling barrier engineering. Specifically, 2D-based FETs are seen as promising candidates for nanoscale dimensions, typically with channel lengths of $\leq$40 nm, which facilitate ballistic or quasi-ballistic transport of carrier.

FETs are fundamental components in contemporary electronic circuits. The FET structure consists of a metal gate, a channel made up of semiconductor between source and drain, and an oxide that acts as a blockade between channel and gate. The current flowing through the channel, known as the drain current (I_D), is produced by the drain voltage (V_D) and can be controlled by adjusting gate voltage (V_G), which alters the functioning of channel. FETs are devices that control the flow of current by using an electric field. Thanks to their small size, FETs are commonly used in integrated circuits, voltage-controlled resistors, logic circuits, and television receivers. The key challenge for silicon-based devices, which are critical to contemporary technological development, lies in the difficulty of continued scaling of dimensions. As thickness of silicon is decreased to a few nanometers, transistor performance degrades significantly due to increased carrier scattering [17]. In contrast, atomically thin 2D semiconductors uphold their properties at subnanometer dimensions and provide potential for the integration of monolithic 3D. This opens the door for a strategic shift, focusing on 2D semiconductors as alternative channel materials to address silicon's scaling limitations.

Numerous 2D materials have been broadly studied for future electronic and optoelectronic applications because of their diverse band gaps, effective electrostatic control, and high carrier mobility. These characteristics, along with tunable electronic properties and mechanical flexibility, enable 2D materials particularly attractive channel materials in highly efficient 2D FETs, suitable for emerging mobile and internet of things (IOT) environments. The collection of key parameters of the device, such as density of carrier, resistivity, contact resistance, mobility, dielectric permittivity, charge trap densities, and the anisotropy in carrier transport and precise characterization of 2D FETs, is important to understand 2D materials and linking them to FET performance. A significant focus of 2D material-based semiconductor research is the development of FETs with high conductivity, low power consumption, high ON/OFF ratios, and elevated carrier mobility. It is crucial to grasp the electrical properties of these devices, as traditional characterization methods may yield unreliable outcomes when employed to ultrathin 2D materials. For instance, in bulk semiconductors, charge density and room-temperature electrical conductivity are directly related. Though, traditional doping techniques cannot be applied to 2D materials because of their atomic thinness. Instead of this, alternative approaches like charge transfer doping are commonly utilized to produce hole and electron carriers. In few-layer materials, charge density drops sharply away from the surface, unlike bulk semiconductors where it remains uniform. Additionally, pristine surfaces of 2D materials form weaker van der Waals bonds with neighboring materials, creating difficulties for achieving low-resistance contacts due to a tunnel barrier that impedes carrier transport. Stronger bonding requires disrupting the crystal structure, leading to defect states [14]. Thus, precise characterization of properties such as metal-semiconductor Schottky barrier and contact resistance is crucial. Interfaces between metals and 2D semiconductors often experience Fermi level caused by the defect-induced interface states, tunnel barrier, and orbital overlap with neighboring materials. Accurate analysis of the Fermi-level pinning and Schottky barrier is necessary, as these factors can significantly increase contact resistance at the interfaces. Several key performance metrics are crucial for evaluating FETs. One important criterion is that a high-quality FET should exhibit a lower subthreshold swing (SS), which is written as follows:

$$\mathrm{SS} = \frac{dV_G}{d\log_{10} I_D} \tag{4.1}$$

FETs function like switches, providing high channel conductivity when in the ON state and low conductivity in the OFF state. Therefore, the current switching ratio is a key parameter in evaluating FET performance. Additionally, mobility plays a significant role in defining the efficacy of higher-performance FETs. In 2D materials, charge carrier transport is restricted to the plane of material. The mobility of carrier is influenced by scattering and is given by:

$$\mu = \frac{e\tau}{m^*} \tag{4.2}$$

where m^* is the effective mass of in-plane electron and τ is the scattering time. The main scattering mechanisms include: (a) electron and phonon scattering; (b) electron and electron scattering and scattering by charged impurities; (c) surface roughness coulomb and phonon scattering; and (d) short range scattering [38,39]. The extent to which these factors impact mobility is assessed using Matthiessen's rule:

$$\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \frac{1}{\mu_3} + \frac{1}{\mu_4} \tag{4.3}$$

Additionally, flicker noise can limit FET performance. This type of electronic noise has a power density spectrum that is indirectly related to frequency. Flicker noise is present in nearly most of the devices, generally linked to channel impurities and to generation/recombination noise in transistors because of memory effects of the base current. To fully understand the latent of 2D material for nanoscale FET design, a comprehensive evaluation of its properties at various length is essential. For this, multiscale simulation has emerged as a vital approach for analyzing, designing, and estimating the performance of FETs based on 2D materials. This strategy effectively bridges different length scales by avoiding the need to treat individual interactions at the atomic level. The fundamental characterization of any material system can be derived from first-principles calculations using density functional theory (DFT). DFT simulations provide an accurate representation of energy dispersion relations (*E*–*k*) of 2D material, enabling the abstraction of critical electronic characteristics such as effective mass, energy band gap, electron affinity, work function and scattering rates [40]. These properties are essential for multiscale simulation frameworks. However, the computational cost of DFT increases dramatically in the system with the atoms number, making it unfeasible for analyzing 2D materials higher than a few hundred atoms. To overcome this limitation, a material Hamiltonian can be used through the tight-binding approximation, which captures relations between lattice neighboring atoms and is described in an atomic orbital basis set. This approach uses a set of fitting parameters to guarantee the DFT simulated E-k relationship of the 2D material. It permits for efficient computation of electronic as well as transport properties such as transmission spectrum and the density of states for larger systems without the complexities of a fully atomistic model. It is significant to note that 2D FET design is still in its initial stages, and comprehensive simulations and experiments are needed to establish the relations between 2D materials, design of device strategies, and fabrication technologies.

4.6 POTENTIAL APPLICATION AREAS OF TMDC MATERIALS

TMDC materials have garnered significant interest owing to their exceptional chemical and physical properties, which are valuable for fundamental research and various applications, including sensing, electronics, energy devices, photonics, etc. The unique characteristics of these layered materials include optical transparency, tunable electronic structures, high sensitivity for sensors, and superior electrostatic efficiency make them highly promising for a range of uses. Their weaker interlayer vdW interactions enable the formation of atomically sharp heterostructures of high

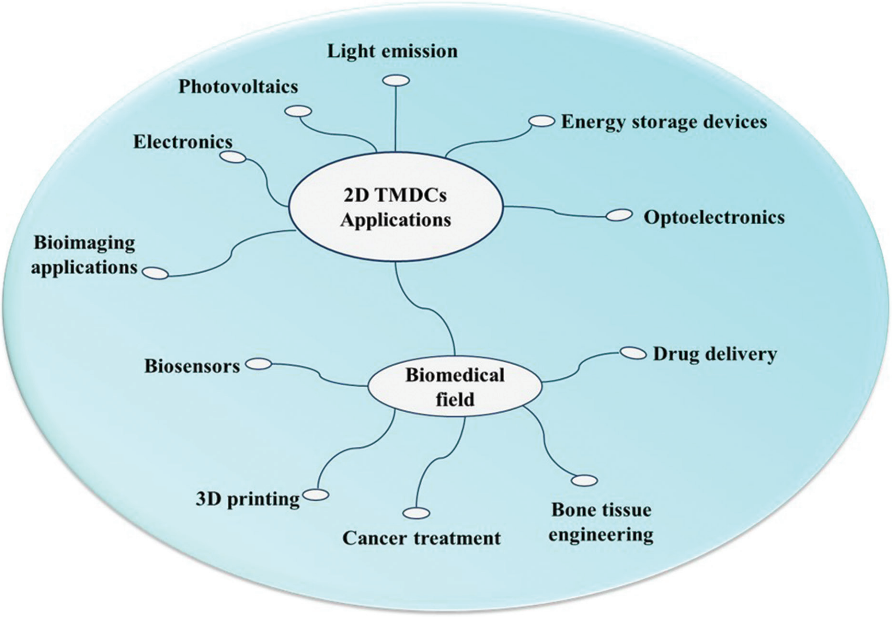
Light emission
Photovoltaics
Energy storage devices
Electronics
2D TMDCs Applications
Optoelectronics
Bioimaging applications
Biosensors
Biomedical field
Drug delivery
3D printing
Cancer treatment
Bone tissue engineering

FIGURE 4.2 Potential applications of 2D TMDC materials.

quality. This section highlights key applications of TMDC materials as shown in Figure 4.2, particularly in biomedical, bioimaging, electronics, optoelectronics, light emission, photovoltaics, and energy devices, etc. The figure illustrates a variety of devices that can be developed using the physical, chemical, and optoelectronic properties of 2D TMDCs.

4.6.1 BIOMEDICAL FIELD

Nearly all impactful and fascinating properties of TMDCs have recently been investigated in biomedical field. These advancements include various approaches that hold potential for future innovations in biomedical field, bridging the gap between laboratory research and clinical applications, ultimately benefiting humanity.

4.6.1.1 Biosensors

A biosensor is designed to identify biological substances and transform their concentrations into measurable signals, which can be electrical, optical, or thermal. These devices are commonly utilized in medical diagnostics, monitoring of environmental pollution and food safety. A typical biosensor comprises two primary components: a signal conversion and a biorecognition unit. Biorecognition process relies on specific interactions, such as antigen–antibody binding, nucleic acid hybridization, and enzyme-catalyzed reactions, to ensure accurate detection of target substance. Signal conversion unit then translates these chemical or physical changes into detectable signals. TMDCs offer an outstanding biocompatibility, a large surface area, and hasty heterogeneous electron transfer, making them suitable for use in biosensors [41]. The band gap of TMDCs can be tuned by modifying the elemental composition, the arrangement of M and X atoms within the 2D layers, and layer's thickness. This tunability leads to adjustable fluorescence and electrochemical properties, making TMDCs ideal for use in biosensors as signal conversion units. Biosensors based on TMDC can be categorized into various types, including FET, electrochemical, chemiluminescence, thermal, fluorescence, colorimetric, etc., allowing for the detection of substances at very lower concentrations.

2D TMDCs allow the immobilization of huge quantities of biomolecules/area, making them ideal for designing high-efficiency biosensors capable of detecting a wide range of analytes, such as glucose, free radicals, DNA, dopamine, RNA, and further reactive oxygen species. An extremely efficient MoS_2-based biosensor is developed for sensitive and label-free detection of prostate-specific antigen, with a detection limit as lower as 1 pg/mL [42]. Additionally, biosensing platforms based on WS_2 and MoS_2 have been created by utilizing peptides as bio-probes for detecting collagen biomarkers [43]. FET biosensors have shown effectiveness in the detection of polar and charged biological samples through electrostatic interactions between dielectric channel and biomolecules [44]. MoS_2 offers a wide array of thicknesses and surface features, and when reduced to very small nanoscale dimensions, it exhibits exceptional photonic absorption properties, which can be customized for recognition of optical antigen. Recently, an innovative ratiometric immunoassay has been developed using ultrafine MoS_2 sheets. This breakthrough paves the way for developing ratiometric immunoassays by employing a single nanocomponent strategy for highly sensitive biomarker detection. Despite advancements in ratiometric biosensors, many systems rely on multicomponent setups with numerous probes and nanoparticles, instead of harnessing the full possibilities of single material. To address this, colorimetric biosensor based on MoS_2 nanosheet is developed for detecting glucose and H_2O_2 [45].

A FET biosensor operates on the principles of a metal-oxide-semiconductor field-effect transistor (MOSFET). It incorporates electrolyte solutions, reference electrodes, and ion-sensitive membranes, identical to the metal gates found in structures of MOSFET. Target biomolecules are adsorbed by the ion-sensitive membrane, which causes changes in electrical signals like channel conductance and leakage current, allowing for detection. FET biosensors provide label-free detecting capabilities, quick reaction times, and excellent sensitivity. Certain single-layer 2D materials have direct band gaps between 1 and 2 eV, making them highly valuable for developing ultra-sensitive FET biosensors as biorecognition units.

4.6.1.2 Drug Delivery

Thin-layer TMDCs possess a range of advantageous characteristics that make them ideal for the applications of drug delivery [46]. For instance, the drug-loading capacity of 2D MoS_2 has been demonstrated to be higher than that of graphene oxide because of the hydrophobic interactions that drive their surface adsorption effects [47]. Targeted drug administration based on imaging can be accomplished with TMDC quantum dots (QDs) such as WS_2 and MoS_2. MoS_2 QDs loaded with thiolated doxorubicin showed good cellular uptake capability and a glutathione

(GSH)-triggered drug release effect in a recent study, suggesting the possibility of simultaneous imaging-assisted drug administration in vivo [48]. Drug delivery using hybrid nanostructures containing lipids has attracted a lot of attention lately. For this reason, liposome conjugates based on TMDC have been investigated. For multiplexed drug delivery, liposome-mediated MoS_2 and WS_2 nanosheets were effectively constructed in one research [49]. Additionally, the work sheds light on how phosphocholine liposomes and TMDC nanosheets interact, laying the groundwork for the creation of another hybrid nanostructures for drug delivery. MoS_2 nanosheets have a higher surface area-to-volume ratio, which makes them highly effective for loading drugs, including photosensitizers, doxorubicin, paclitaxel, and 7-ethyl-10-hydroxycamptothecin. To extend their circulation time, TMDC materials are often coated with PEG-like surface functionalizing ligands before the drug loading [50]. MoS_2 and other TMDC materials hold considerable potential as gene delivery platforms. Drug molecules may readily bond to the chalcogens by straightforward reactions because of the TMDCs' sandwich structure, in which chalcogen atoms surround metal atoms. TMDCs are superior options for targeted gene/drug delivery and sustained gene/drug release than graphene and its derivatives.

4.6.1.3 3D Printing

Another emerging perspective regarding TMDC family materials is their potential to replace traditional three-dimensional printing inks. Nontoxic, water-based inks have been developed using cleansed 2D materials. In a study, the authors established the successful preparation of 3D printable inks with MoS_2 nanosheets, resulting in mechanically robust and chemically stable materials [51].

4.6.1.4 Cancer Treatment

In the world of biomedicine, multimodal imaging has enormous potential thanks to the emergence of nanomaterials based on TMDCs. 2D TMDC nanosheets that have been fluorescently labeled can be employed for imaging purposes, while TMDC QDs, such as MoS_2 and WS_2 QDs, possess high, stable fluorescence and little photobleaching tendencies, which allow for their usage even in the absence of fluorescent labeling. The effectiveness of TMDC nanoparticles as agents for imaging modalities like magnetic resonance imaging, computed tomography (CT), positron emission tomography, photoacoustic imaging, and single-photon emission CT is further improved by doping with paramagnetic particles [52]. Recently, biodegradable SiO_2-doped ultrasmall MoS_2 nanodots were created for photodynamic treatment and dual-mode CT imaging-guided photothermal therapy for invasive tumors [53].

TMDC-based materials are anticipated to offer novel, biocompatible nanosystems for theranostics and multimodal imaging. Another promising option for a highly effective nanoplatform in cancer therapy directed by multimodal imaging is degradable VS_2. Particularly for photothermal therapy (PTT), an invasive technique that utilizes an external laser, usually in the near-infrared range, to induce hyperthermia within the tumor, these 2D materials are beginning to show promise as a viable alternative in modern oncology [54]. PTT can directly damage tumor tissues by inducing apoptosis or changing gene expression and protein synthesis. Photodynamic therapy (PDT), a nominally invasive, clinically accepted treatment, works by using near-infrared (NIR) light to activate photosensitizers in the existence of oxygen, producing cytotoxic reactive oxygen species (ROS) that destroy tumor cells and stimulate immune responses [55]. However, PDT is often limited by poor deep tissue penetration and the hypoxic situations of tumor microenvironment, which hamper the creation of singlet oxygen species. Combining PTT with PDT can improve outcomes, as the hyperthermia from PTT enhances blood flow and the delivery of oxygen to tumor sites. TMDC materials, with their tunable size, larger surface area, and optical properties, are projected as appropriate photosensitizers for PDT. Their enhanced permeability and retention effect also make them useful for tumors photoacoustic imaging. Due to their litheness, ease of surface modification, and higher NIR absorption efficiency, TMDC materials are well-suited for cancer theranostics.

A newer green therapy for tumors is microwave hyperthermia, which has drawn interest in addition to PTT. It lessens the negative side effects of radiation and conventional chemotherapy [56]. Microwave hyperthermia employs radiofrequency to produce quicker heat production, deeper tissue penetration, and shorter irradiation periods than PTT, which uses NIR light. High temperatures during microwave ablation, however, have the potential to hurt and harm healthy tissues. Recent research on nanomaterials, including TMDCs, has identified them as suitable candidates for microwave-activated heating, minimizing these destructive effects. Radiotherapy (RT), though effective, is invasive and can cause radiation-induced tissue damage. Radiosensitizers, typically containing heavier metals with higher atomic numbers, enhance radiotherapy by increasing deposition of energy in tumor cells and promoting the release of Auger and secondary electrons, which induce DNA damage and tumor suppression [57]. Immunotherapy, a treatment modality that stimulates the body's immune system to fight cancer, has become the fourth major cancer treatment after surgery, radiotherapy, and chemotherapy [58]. It offers durable antitumor effects and reduces metastasis, positioning it as a critical strategy in modern cancer treatment.

4.6.1.5 Bone Tissue Engineering

Bone tissue engineering and scaffolds for bone regeneration are always needed. For this goal, a variety of osteoinductive materials have been investigated; however, TMDC-based compounds have garnered a lot of attention lately. TMDC materials can be used to create biocompatible scaffolds with impressive regenerative potential. In one study, a bifunctional scaffold with photothermal therapeutic potential was created by growing MoS_2 nanosheets on the bioceramic material surface [52]. This scaffold presents a viable therapeutic approach for the cure of tumor-induced bone abnormalities by efficiently promoting the development and proliferation of osteogenic bone marrow mesenchymal stem cells (BMSCs).

4.6.2 BIOIMAGING APPLICATIONS

Bioimaging is one of the most direct and effective techniques for studying biological structures and functions, such as cells, tissues, organs, and the human body, using optical or electronic microscopy. It plays a crucial role in revealing physiological processes and aiding in the treatment and diagnosis of several diseases. Bioimaging techniques include magnetic resonance imaging (MRI), fluorescence imaging (FI), CT, Raman imaging (RI), photothermal imaging (PTI), ultrasound imaging (USI), multimodal imaging (MMI), and photoacoustic imaging (PAI), which combine multiple imaging technologies [41]. Current research trends in bioimaging materials focus on two main areas: combining bioimaging with therapy and integrating different bioimaging methods to enable multimodal imaging. TMDCs are primarily utilized as contrast agents in MRI, FI, CT, MMI, and PAI applications.

4.6.3 ELECTRONICS

While TMDCs have been researched for many years in a variety of applications, new developments in the production of nanoscale devices have opened new avenues for nanoelectronics. TMDCs such as $MoSe_2$, MoS_2, WSe_2, and WS_2 have size-tunable band gaps, which at the single-layer (SL) level change from indirect to direct, making them perfect for application in electroluminescent devices, photodetectors, transistors, and diodes. High-performance flexible electronics is the most latent near-term uses for 2D TMDCs-based semiconductor. The key breakthroughs in TMDC-based electronics are in transistor fabrication, which holds great potential for digital electronics.

SL MoS_2 has undergone mechanical testing that has shown it to be 30 times stronger than steel and capable of up to 11% deformation before failing [59]. Given its strength, MoS_2 is an excellent choice for flexible substrates as it is one of the best semiconducting materials. It has been shown that gas sensors [60] made of exfoliated MoS_2 and electrochemically lithiated as well as CVD-grown MoS_2 in combination with an ionic gel gate dielectric may produce flexible transistors [61]. The mechanical characteristics of other dichalcogenide semiconductors are similar to those of MoS_2. Semiconducting 2D TMDCs coupled with different 2D materials like insulating boron nitride (BN) and conducting graphene can make hybrid 2D electronics on flexible substrates. These materials offer a promising alternative to silicon-based transistors due to their tunable bandgap ultrathin structure, providing high current switching ratio that enhances the flexibility and transparency of devices. TMDC nanosheets, such as MoS_2, exhibit faster switching in comparison to conventional 3D electronic materials, resulting in a considerable reduction of power dissipation and SCEs. They are great candidates for use as channel materials in FETs because of their absence of dangling bonds, high structural stability, and electron mobility.

4.6.4 OPTOELECTRONICS

Direct-bandgap semiconductors like monolayer (ML) MoS_2 and other TMDCs have exceptional qualities that make them ideal for fabricating optoelectronic devices. Electronic systems with the ability to produce, detect, employ, or control light are known as optoelectronic devices. The potential of nanomaterials including semiconductor QDs, carbon nanotubes, and nanowires in optoelectronic applications such as photodetectors, displays, LEDs, lasers, solar cells, and optical switches has been thoroughly studied [62]. It is projected that transparent and flexible optoelectronic devices will play a bigger role in transparent displays, wearable electronics, and solar arrays. The capacity of semiconductors to absorb and emit light is largely dependent on their electronic band structures. Photons with the energy above the bandgap can be absorbed or emitted by semiconductors having a direct band gap. Conversely, those with an indirect band gap have a less effective mechanism for photon absorption or emission since they need to absorb or emit an extra phonon to make up for the momentum difference. SL TMDCs have a lot of potential for optoelectronic applications since they primarily have direct band gaps [26]. Their potential for flexible and transparent optoelectronic devices is further enhanced by their atomically thin and processable nature [63].

Applications range from highly sensitive, lesser noise phototransistors to solar cells and light-emitting diodes (LEDs). In addition to their electronic and optoelectronic capabilities, TMDCs possess intriguing mechanical properties, with ML MoS_2 being as rigid as steel, making them ideal for flexible electronics. Processable TMDC nanosheets that are atomically thin can satisfy the increasing need for flexible and transparent optoelectronic devices, including transparent displays, solar panels, and wearable electronics [63]. For instance, using MoS_2, a p-n junction diode has been built, proving that stable p-n junctions may be created in liquid-gated ambipolar transistors. Similar performance has been observed with WSe_2 nanosheet-based p-n junction diodes. LEDs are another promising application for TMDC compounds, pointing to future advancements in both electronics and optoelectronics.

4.6.5 LIGHT EMISSION

Photoluminescence and Electroluminescence are two key groups of light emission. Photons that generate light in response to an electrical stimulation are known as electroluminescence, and this property is helpful in optoelectronic devices like diode lasers and LEDs. On the other hand, photoluminescence occurs when a substance absorbs a photon and then reemits it, occasionally at a different energy level. In contrast to indirect-bandgap semiconductors, direct-bandgap semiconductors allow for the far more efficient radiative recombination of electrons and holes to create photons [63]. Graphene requires chemical treatments due to lack of bandgap, to create localized bandgaps that can display photoluminescence; in contrast, ML semiconducting TMDCs have direct bandgaps, which makes them excellent candidates for the active light-emitting layer in future flexible optoelectronics [64]. Photoluminescence is demonstrated by ML MoS_2, which has a direct band gap and a substantially larger quantum yield than both bilayer and bulk MoS_2. But before any useful optoelectronic devices can be created, a great deal of work needs to be done to comprehend the mechanisms underlying photoluminescence emission and quenching processes. This is because the quantum yield of photoluminescent measured in MoS_2 thus far is still lesser than predictable for a direct-gap semiconductor.

4.6.6 PHOTOVOLTAICS APPLICATIONS

TMDCs are attractive prospects as light-absorbing materials for substitution of thin-film solar cells, which may be applied to buildings and curved surfaces, due to their relative abundance on Earth and their direct band gaps in visible spectrum [65]. Several TMDCs exhibit well-aligned work functions and band edge levels with electrode materials that are frequently utilized. Additionally, the capability to modify TMDCs bandgap using several intercalants, for instance, organic molecules and metal ions, might enable the tuning of optical absorption for photovoltaic applications. TMDCs have shown to play a few functions in photodetectors and photovoltaics. WS_2 and MoS_2 thin films are photosensitive, and phototransistor built from single MoS_2 layer has demonstrated potential for photodetector. This device has a strong photoresponsivity, alters its photocurrent according to the intensity of incident light, and reacts to variations in light levels in less than 50 ms [66]. Different thicknesses of MoS_2 layers can be used to adjust photodetection for various wavelengths.

Strong light interactions, adjustable optical bandgaps, and remarkable structural, surface, and electrical features of atomically thin 2D materials are driving much research in the field of energy-harvesting devices. Using less active absorber material, these materials also allow for extremely efficient solar energy conversion. Innovative solar systems can be made easier by the visible spectrum band gaps of TMDCs, which range from metallic to insulating [67]. Approximately 1%–5% of incident sunlight may be absorbed by semiconducting SL TMDCs with thicknesses less than 1 nm, such as MoS_2, $MoSe_2$, and WS_2. This performance is in close alignment with that of interfaces of organic/organic solar cell. Such materials exhibit a far greater capacity to absorb sunlight than traditional semiconductor materials such as Si and GaAs. The photovoltaic effect is caused by the separation of photogenerated electron–hole pairs, which is made possible by the connection of two materials with opposite charge carriers seen in a conventional solar cell.

4.6.7 ENERGY STORAGE DEVICES

The atomically thin layered structure, large surface area, superior electrochemical characteristics, and effective ion-electron migration of 2D TMDCs are drawing a lot of interest as electrodes for energy storage applications, such as supercapacitors and lithium-ion batteries (LIBs) [68]. While retaining structural stability at the time of charging and discharging cycles, these layered architectures provide additional locations for ion occupancy. Rechargeable energy storage methods for portable electronic gadgets that are greatly sought after are Li-ion batteries [69]. While graphite has traditionally been utilized as the anode material in LIBs, its limited capability to hold lithium ions for higher power consumption has led to the selection of TMDC materials as a viable alternative. Another popular substitute for LIB is sodium-ion batteries (SIBs) [70]. But since they cannot hold enough Na^+ ions, carbon-based anodes are not good for SIBs. The recognition of TMDCs as effective substitute anodes for SIBs is consequently growing. The high inherent capacitance of TMDC-based electrodes at high current intensities makes them useful for supercapacitor designs as well.

4.7 CHALLENGES AND FUTURE DIRECTION

4.7.1 CHALLENGES

In silicon-based technologies, downscaling has grown more challenging because of intrinsic device limits and process limitations. Prominent semiconductor firms are currently exploring the possibility of extending Moore's Law through the usage of 2D materials. One goal of basic research on 2D materials at the device level is to show how these materials may be optimized for better performance [14]. Examples of such research include material growth, contact resistance optimization, dielectric integration, and device miniaturization. For instance, Intel has effectively demonstrated and characterized the direct metal-organic CVD of 2D materials using a 300-mm silicon platform [14,63]. A 2-inch sapphire wafer has been covered by Taiwan Semiconductor Manufacturing Company Limited (TSMC's) report on the development of single crystal h-BN MLs on a copper sheet. To put 2D channel FETs in line with the newest silicon technology, Intel has also investigated scaling them down to a source-to-drain contact spacing of 25 nm. Alternatively, continuous efforts are directed toward verifying the fabrication of 2D materials scalability and compatibility with silicon-based production lines.

Several important issues must be resolved before such devices may be more widely used. There has been discussion of the many difficulties involved in creating electronics based on 2D TMDCs. We need to draw attention to three important issues: doping; low-resistance connections and industry-compatible high-dielectric constant. Due to the frequency of point defects in 2D TMDCs, such as iso-valent impurities and charged chalcogen vacancies, which are related to electronic device performance but have not received much discussion [40,71]. Device features include on-state current, threshold voltage fluctuation, and mobility are negatively impacted by these faults. For optics and photonics, point defects in these materials have less impact, but for electronics, reducing fault concentration is essential. However, electrically driven luminescence yields are usually below a few percent because of carrier recombination, scattering, and weak contacts, even though photoluminescence quantum yields of 100% may be attained in 2D TMDCs. Carriers can be concentrated as high as $10^{12}/\text{cm}^2$ in 2D TMDCs that are chemically vapor-deposited or mechanically exfoliated due to charged chalcogen vacancies [23,71]. It is more difficult to modify the carrier concentration by substitutional doping because of this starting concentration and the existence of neutral impurity atoms. The formation of efficient connections is further hampered by the challenge of doping 2D TMDs. While n- and p-type connections in silicon are achieved by using degenerately doped areas, the same methods do not work for 2D TMDCs. In addition, interactions between charges in the dielectric are facilitated by the high concentration of chalcogen vacancies, which can result in the development of interface states and accidental doping from the substrate.

The primary challenge in advancement of 2D TMDCs is achieving low-defect, wafer-scale synthesis as it is essential for creating intrinsic channels and efficient doping schemes. The production of higher-performance FETs depends on the establishment of clean van der Waals interfaces between semiconductors and dielectrics as well as between and semiconductors and metals. A high-k dielectric that is compatible with complementary metal-oxide-semiconductor (CMOS) technology and does not adversely affect the performance of 2D TMDC channels is required. Any improvements in device performance must also include stability, scalability, and industrial compatibility to make sure that the innovations are effective, repeatable, and appropriate for broad adoption.

4.7.2 Future Direction

Layered TMDCs have been known about and researched for many years, their atomically thin, 2D forms represent a very new and intriguing area of nanotechnology with a wide range of potential uses in optoelectronics and nanoelectronics. Many members of the TMDC family have large band gaps that make them desirable as channel materials in logic transistors, and some SL TMDCs have direct band gaps that provide great potential for optoelectronic applications. 2D MoS_2, for example, has been used as gas and chemical sensors as well as a demonstration platform for transistors with remarkable current switching ratios and integrated circuits that can perform logic operations. Notable occurrences have also been noted, including a significant spin–orbit effect and valley polarization. Researchers may take use of earlier research on the embolism chemistry, characterization, and materials processing of bulk TMDCs, as well as device manufacturing and nanoscale characterization methods created for carbon nanotubes and graphene, by investigating the physics and chemistry of 2D TMDCs [72]. Nevertheless, as research continues, novel and intriguing applications are probably going to surface since 2D TMDCs have a lot of special qualities that are not present in other material systems. Progress in this area will be reliant in the years to come on large-scale, reproducible sample preparation methods that produce homogenous, atomically thin TMDC films in solution or on substrates. Controlling the thickness and area of chemically or exfoliated produced flakes, as well as developing novel techniques and materials to generate these materials safely and effectively in large quantities, is a problem in solution-phase preparation. Meanwhile, to attain enormous areas, larger grain dimensions, homogeneity, and accurate control over the number of layers, advances in crystal growth techniques are needed for the fabrication of solid-state samples [73]. More researchers will be able to investigate a broad variety of applications and obtain better understanding of the chemical and physical features of TMDCs with the availability of high-quality samples. Research on 2D TMDC materials is an emerging and rapidly advancing field that holds significant promise for future developments, despite being relatively underexplored at this stage.

4.8 CONCLUSION

In this work, the promising aspects of new 2D material TMDC have been explored for various device applications. We have very closely studied the two approaches of material synthesis, namely top-down approach and the bottom-up approach. Out of all the synthesis techniques, it was found that CVD method is the most effective technique for good-quality layers of TMDCs. Also, it was observed that atomistic level of synthesis of TMDCs is also proving to be in line with requirement. Keeping in view the applications of the TMDCs, we have studied here the optical and electronic properties of the material as well. It was also observed that the material has promising use in optoelectronics. The layered structure of the material has also been explored, taking into consideration the usage of the material in FETs. All the possible application areas, namely electronic device, optoelectronic devices, and biochemical area, have been explored explicitly. A special emphasis on TMDCs use in FET devices has been vividly studied. Moreover, the possible challenges in the 2D TMDC material have been also presented here in this chapter. Finally, various future aspects of the material have also been explored to emphasize the broadened usability of the material.

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5 From Classical to Quantum

Ballistic Transport in Nanosheet FETs

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5.1 INTRODUCTION

Moore's Law has spurred the increasing downsizing of semiconductor devices, resulting in extraordinary advances in electronic component performance and efficiency [1–3]. As classic transistor layouts reach their physical limits, the semiconductor industry is looking into new transistor designs to suit the growing need for high-speed, low-power electronics. One of the most promising advancements in this field is the nanosheet field effect transistor (FET), which provides greater electrostatic control and scalability than traditional planar transistors [4,5]. The development of nanosheet FETs represents a huge step forward in semiconductor technology. These devices have a vertically stacked nanosheet structure, which allows for more control over the channel via which current flows [6]. These transistors' nanoscale dimensions and unique construction give them various advantages over typical FETs, including reduced short-channel effects and enhanced performance measures such as subthreshold swing and threshold voltage. Furthermore, their ability to integrate in three dimensions (3D) makes them a very appealing option for modern integrated circuits and future nanoelectronics.

As device dimensions reduce to the nanoscale, quantum mechanical phenomena become more relevant in charge carrier behavior within the channel. Classical models, which assume diffusive transport driven by scattering events, are unable to describe the entire dynamics of electron transport at these small scales. Instead, the ballistic transport model provides a more accurate depiction, particularly in devices where the mean free path of carriers is equal to or greater than the device length, allowing electrons to pass down the channel without scattering.

Ballistic transport is a non-scattering charge transport mode in which electrons pass through the channel unhindered by phonons or contaminants. This phenomenon is especially significant in nanosheet FETs, where the channel length is on the order of nanometers. In this regime, quantum concepts like as wave-particle duality and conductance quantization govern the device's transport properties rather than classical diffusive mechanisms. As a result, these devices' current–voltage (I–V)

DOI: 10.1201/9781003543923-5

properties differ dramatically from what traditional theories predict. To adequately understand and optimize the performance of nanosheet FETs, models that account for both quasi-ballistic and ballistic transport regimes must be used. The Landauer technique provides a useful framework for understanding this transport in terms of conductance quantization and electron transmission probability through the channel. The Landauer approach allows us to precisely simulate critical nanosheet FET performance factors such as drain current, subthreshold slope, and threshold voltage.

This chapter investigates ballistic transport mechanisms in nanosheet FETs, bridging the classical and quantum transport models. We will look at the device structure, the transport features that are specific to these transistors, and how ballistic transport affects their overall performance. In particular, we will investigate how the quantum behavior of electrons might be used to improve the performance of nanosheet transistors, particularly in terms of speed and power efficiency. This chapter seeks to provide a full knowledge of nanosheet FETs and their prospective applications in the next generation of high-performance electronics by combining theoretical models, simulation results, and experimental validations. The transition from classical to quantum transport opens up new possibilities for device design, allowing the development of transistors that can work efficiently at ever-smaller scales.

5.2 DEVICE STRUCTURE OF NANOSHEET FETS

Nanosheet FETs have a novel structure that differs from standard planar transistor designs, providing greater channel control and scalability for advanced semiconductor nodes [7]. A nanosheet FET's stacked-sheet construction allows for many conduction channels and enhanced electrostatic control. This section will go over the basic components and structural aspects of nanosheet FETs, compare them to earlier generations of transistors, and discuss their benefits in the context of current electronics.

5.2.1 Basic Structure Overview

The vertically stacked nanosheet channel is crucial to the nanosheet FET, with each sheet serving as a distinct charge carrier conduction pathway. These sheets are commonly made of silicon (Si) or silicon germanium (SiGe) [8,9] as shown in Figure 5.1, with thin dielectric layers between them [10]. The total structure can be defined as a three-dimensional (3D) multi-channel architecture as shown in Figure 5.2, with the channels encased in a gate material that provides tight control over electron flow. Multi-channel [11] configuration is also possible in nanosheet FET structure.

The significant elements of the nanosheet FET structure: In a nanosheet FET structure, certain critical elements work together to enhance the device's performance. At each end of the channel, there are source and drain contacts, which play a vital role in the movement of charge carriers. The source allows these carriers to enter the channel, while the drain enables them to exit, maintaining a steady flow of current through the device. The heart of this structure lies in the nanosheet channels, where conduction occurs. These channels consist of several ultrathin sheets stacked vertically, often just a few nanometers thick. By adjusting the width of these nanosheets,

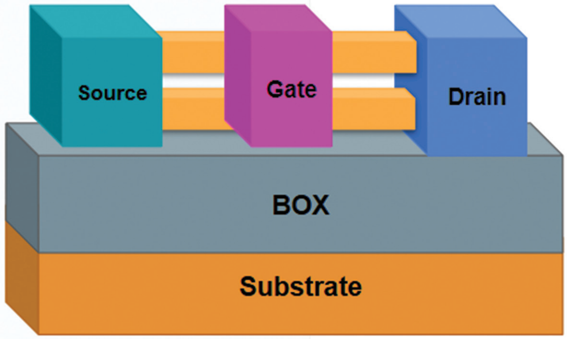

FIGURE 5.1 Cross-sectional view of vertically stacked $Si_{0.2}Ge_{0.8}$ nanosheet tunnel FET.

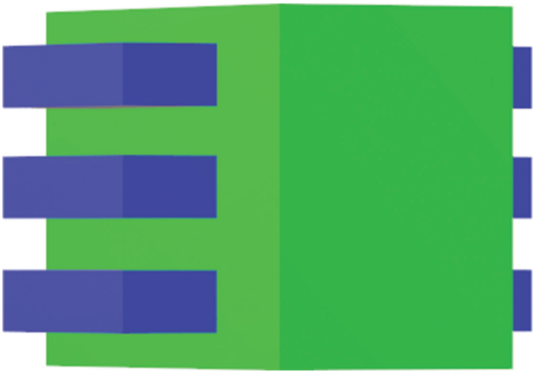

FIGURE 5.2 Cross-sectional view of nanosheet nFETs with HfO_2 gate dielectric.

engineers can fine-tune how the device performs, offering flexibility based on the application. At the core of the device's configuration is the gate-all-around (GAA) design. Unlike traditional structures, the gate material here completely wraps around the nanosheets. This surrounding gate provides superior electrostatic control, which is key to minimizing short-channel effects—a common challenge in smaller devices. Additionally, dielectric layers made of high-k materials like hafnium oxide (HfO_2) are strategically placed between the gate and the channel. These thin dielectric barriers serve to insulate the gate, reducing unwanted leakage currents and ensuring that the device operates efficiently, even at the nanoscale.

5.2.2 GATE-ALL-AROUND (GAA) DESIGN

The GAA architecture is a distinguishing feature of nanosheet FETs, representing advancement from previous transistor designs such as fin field-effect transistors (FinFETs) [12–14]. In FinFETs, the gate wraps around three sides of the channel (triple-gate structure), whereas in nanosheet FETs, the gate completely surrounds each nanosheet channel. This entire gate encasement improves electrostatic control

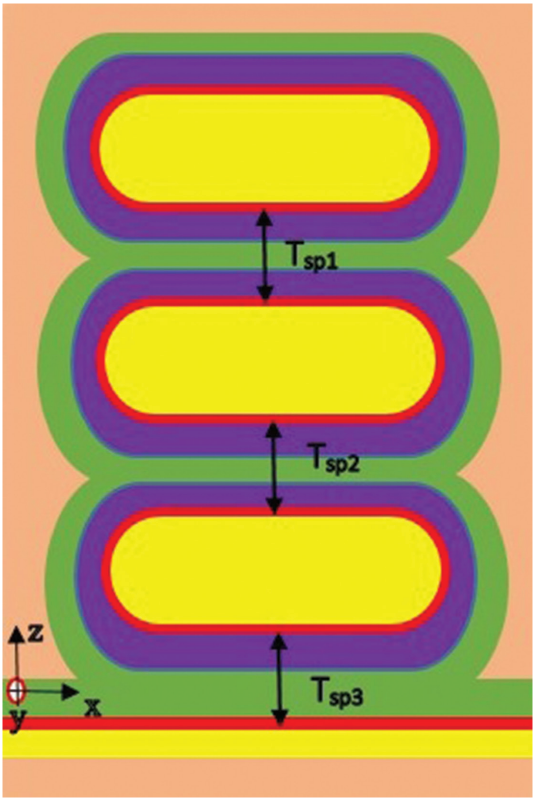

FIGURE 5.3 The structure of three stacked gate-all-around nanosheet FET.

in the channel, lowering leakage current and increasing on/off ratio. The structure of three stacked GAA nanosheet FET is shown in Figure 5.3. The GAA architecture offers several key advantages [15,16], making it ideal for ultra-scaled transistors. Its design provides superior electrostatic control, allowing the gate to fully modulate the channel and improve performance, especially at very short channel lengths. This results in reduced short-channel effects, such as drain-induced barrier lowering (DIBL) [17,18] and threshold voltage roll-off, which are prominent in traditional FETs as devices shrink. Additionally, the ability to stack multiple nanosheets in the GAA configuration increases the effective channel width, leading to higher drive current compared to planar and FinFET designs, making GAA highly scalable for future technology nodes.

5.2.3 Channel Material Selection

While silicon has generally been the material of choice for semiconductor devices, nanosheet FETs provide channel material flexibility, allowing for the incorporation of high-mobility materials such as silicon germanium (SiGe) or III–V compounds. These materials have better electron and hole mobility than silicon, which improves overall device performance, especially switching speed and power consumption. Silicon nanosheets are still a common choice for nanosheet FETs due to their compatibility with current semiconductor fabrication techniques. However, when devices shrink to the nanoscale, carrier mobility in silicon may become a performance bottleneck. To overcome this, silicon germanium (SiGe) nanosheets [8,19] are frequently used, particularly in p-type FETs, because they provide better hole mobility than pure silicon. This increased mobility leads to better balanced performance in complementary metal-oxide-semiconductor (CMOS) circuits. Materials from the III–V compound family, such as indium gallium arsenide (InGaAs) [20] or gallium nitride (GaN), offer much better electron mobility in n-type FETs. This increased mobility enhances the performance of nanosheet FETs, making them ideal for sophisticated electronic applications.

5.2.4 Nanosheet Geometry and Channel Dimensions

The performance of nanosheet FETs is heavily influenced by the geometry and dimensions of their channels. Key variables include nanosheet width, which influences drive current—wider sheets boost current but may impair electrostatic control. When the nanosheet thickness is reduced to a few nanometers, electrostatic control improves, but at the expense of increased resistance and quantum confinement effects. Furthermore, increasing the stacking density of nanosheets improves total channel width and device performance without enlarging the footprint; however, this necessitates extremely accurate fabrication to assure uniformity.

5.2.5 Source/Drain Engineering

Source/drain engineering in nanosheet FETs [21] is critical for reducing contact resistance and increasing carrier injection. Raised source/drain regions are a typical strategy for reducing parasitic resistance and increasing current flow. Furthermore, utilizing low-resistance materials at the metal–semiconductor interface, such as nickel silicide, improves electrical conductivity and thus device performance. This enhancement promotes faster operation and lower power consumption, making it essential for advanced nanosheet FET designs.

5.2.6 High-k Dielectric and Metal Gate

Combining high-k dielectric materials like HfO_2 with metal gates improves electrostatic integrity and reduces gate leakage in nanosheet FETs. This combination is critical for achieving low leakage currents, particularly at very small channel lengths. High-k dielectrics have a higher dielectric constant than standard SiO_2, which improves gate control and reduces leakage without increasing the gate oxide layer thickness. The use of metal gates, such as tungsten (W) or titanium nitride (TiN), improves device performance by lowering gate resistance, which increases transistor switching speed. These advancements ensure that nanosheet FETs keep their great performance as transistor size reduces in advanced semiconductor technologies.

5.2.7 Fabrication Challenges and Techniques

The fabrication of nanosheet FETs [22,23] involves various hurdles, including the need for enhanced lithography and etching procedures to correctly specify the nanosheet dimensions and alignments. Extreme ultraviolet (EUV) lithography is required for precision patterning, allowing the fabrication of sub-10 nm features crucial for nanosheet FETs in cutting-edge technological nodes (e.g., 3 nm or less). To create the stacked nanosheet structure, selective epitaxy is used to produce layers with certain material properties, such as mixing SiGe and Si for improved performance. Furthermore, anisotropic etching is employed to accurately form and vertically stack the nanosheets, assuring structural integrity throughout the production process, despite the challenges of operating at such small sizes.

5.2.8 Comparison to FinFETs

Nanosheet FETs are viewed as the inevitable successor to FinFETs, as they provide better electrostatic control and scalability [24,25]. Unlike FinFETs, which have a fin-shaped channel, nanosheet FETs have stacked horizontal nanosheets, allowing for a wider effective channel width within the same device size. This design improves gate control, reduces leakage, and boosts performance, especially at smaller geometries. FinFETs suffer limits as device dimensions approach 5 nm, primarily due to short-channel effects and issues expanding the fin width further. Nanosheet FETs, on the other hand, address these concerns through improved scalability and GAA control, making them an attractive candidate for future semiconductor technologies. The nanosheet architecture, with its GAA arrangement and ability to stack numerous nanosheets, provides outstanding performance, establishing it as a key technology for next-generation integrated circuits.

5.3 TRANSPORT MECHANISM OF NANOSHEET FETs

The transport mechanism of nanosheet FETs is critical to determining overall performance, especially when devices scale to nanoscale dimensions. The small size of nanosheet transistors emphasizes quantum mechanical phenomena and ballistic transport, challenging established charge transport models. This section investigates charge carrier transport in nanosheet FETs, focusing on the transition from classical diffusive to quasi-ballistic and ballistic regimes, as well as the impact of the device's structural properties on transport phenomena.

5.3.1 Classical vs. Quantum Transport

As device dimensions decrease, the traditional diffusive model of charge transport [26], which is regulated by scattering events (with impurities, phonons, and so on), fails to characterize the behavior of charge carriers. At nanoscale scales, electrons can flow down the channel with little scattering, signaling the start of ballistic transport.

Classical Transport: In larger transistors, carrier motion is largely diffusive, with electrons experiencing numerous scattering events that may be explained using drift-diffusion models. This mode of transport follows Ohm's Law, which indicates that the current is directly proportional to the voltage and inversely proportional to the resistance.

Quantum Transport: As the channel length approaches the electron mean free path (the average distance an electron travels prior to scattering), quantum processes take over the transport mechanism. Nanosheet FETs exhibit quasi-ballistic or ballistic transport due to their short channel lengths. The current is no longer entirely determined by scattering events, but rather by the likelihood of electron transmission down the channel, as represented by quantum mechanical models [19,27].

5.3.2 BALLISTIC TRANSPORT IN NANOSHEET FETs

In the ballistic transport regime [28,29], electrons move from source to drain in a straight line, without scattering. The channel length of nanosheet FETs is frequently on the order of a few nanometers, which is comparable to or less than the carriers' average free route. As a result, ballistic transfer becomes the primary mechanism.

The carrier mean free path plays a critical role in deciding whether ballistic transport occurs in nanosheet FETs. It denotes the average distance an electron can travel before encountering substantial scattering events, which in nanoscale devices is usually on the order of a few nanometers. When the channel length of the nanosheet FET is shorter than or equal to the mean free route, electrons can travel from source to drain with minimum scattering, allowing for ballistic transport. Ballistic transport has a substantial influence since it allows for quicker electron flow through the channel, which results in greater drive currents and switching rates. Additionally, reduced scattering reduces energy dissipation from resistive losses, resulting in increased power efficiency. This makes ballistic transport ideal in nanosheet FETs, especially for applications that require high-speed and energy-efficient performance.

5.3.3 QUASI-BALLISTIC TRANSPORT AND SCATTERING EFFECTS

In practice, most nanosheet FETs operate in the quasi-ballistic domain, which combines ballistic and diffusive transport modes. Some electrons flow ballistically, whereas others scatter due to phonons, contaminants, or surface roughness at nanosheet interfaces.

Quasi-ballistic transport [30–33] happens when part of the charge carriers in a nanosheet FET move ballistically but still scatter. This results in a hybrid of ballistic and diffusive transport, with most electrons moving without scattering but occasionally colliding, disrupting the ideal ballistic flow. This transport regime is frequent in nanosheet FETs due to their nanoscale dimensions, which reduce scattering but do not completely eliminate it. The primary scattering mechanisms in quasi-ballistic transport are: *Phonon scattering* occurs when electrons interact with lattice vibrations, altering their course and lowering transport efficiency. *Impurity scattering* is caused by imperfections or impurities in the material, which create barriers to electron transport and disrupt ballistic motion. *Surface roughness scattering* [34,35] is especially noticeable in nanosheet FETs, where the narrow channel dimensions make the contact between the channel and gate dielectric more likely to have uneven surfaces, further impeding smooth electron transport. While scattering events do occur, they are minimized in quasi-ballistic transport, allowing the device to perform better than fully diffusive transport.

5.3.4 LANDAUER APPROACH AND QUANTUM CONDUCTANCE

To accurately describe the transport mechanism in nanosheet FETs, especially in the ballistic and quasi-ballistic regimes, the Landauer technique [28] is used. This model treats the channel as a quantum conductor and connects current through the device to electron transmission probability.

Landauer Formula: The current in a ballistic transistor is proportional to the number of conduction channels and the probability that an electron will transmit through the channel from source to drain. Mathematically, the current (I) is given by [28]:

$$I = \frac{2q}{h} \int_{-\infty}^{+\infty} T(E) M(E) f_S(E) - f_D(E) dE \tag{5.1}$$

where q is the electron charge; h is Planck's constant; $T(E)$ is the transmission coefficient; $f_S(E)$ and $f_D(E)$ are the Fermi–Dirac distribution functions for the source and drain, respectively; and $M(E)$ is the number of channels.

Quantum Conductance: In ballistic transport, the conductance is quantized and can be expressed in units of the quantum of conductance, $G_0 = (2q^2)/h$. The total conductance is determined by the number of available conduction modes and the transmission probability.

5.3.5 INFLUENCE OF DEVICE GEOMETRY ON TRANSPORT

The shape of nanosheet FETs has a significant impact on the transport mechanism, specifically the thickness and width of the nanosheet channels, as well as their spacing. Thinner nanosheets provide improved electrostatic control, reducing leakage currents and improving overall device performance. However, if the nanosheets grow too thin, quantum confinement phenomena may occur, modifying the electronic band structure and influencing charge transport capabilities. Wider nanosheets, on the other hand, have a bigger cross-sectional area for electron flow, which results in a higher on-state current. Nonetheless, broader sheets may limit the gate's ability to efficiently control the channel, making the device more susceptible to short-channel effects. The channel length is also an important factor in influencing the transport regime. Shorter channels are more likely to have ballistic transport, which means electrons flow with little scattering. Longer channels, on the other hand, undergo more scattering events, resulting in diffusive transport and a reduction in electron flow efficiency. Thus, improving the geometry of nanosheet FETs is essential for achieving high-performance transport properties.

5.3.6 IMPACT OF HIGH-K DIELECTRIC AND METAL GATE ON TRANSPORT

The use of high-k dielectrics and metal gates in nanosheet FETs improves electrostatic control and reduces gate leakage, but it also affects the transport mechanism. High-k dielectrics, such as hafnium oxide (HfO_2), have a higher dielectric constant, which improves the gate's ability to regulate the channel, allowing better performance at shorter channel lengths. However, the quality of the dielectric interface is critical in this design. Surface roughness or flaws at the interface might cause extra scattering, reducing the ballistic nature of electron transport and lowering performance.

The use of metal gates, such as tungsten or titanium nitride, reduces gate resistance, increasing the device's switching speed. However, these metal gates alter the work function, influencing the channel's electrostatic potential. This change can have an impact on transport qualities, potentially changing the balance between ballistic and diffusive transport, depending on the overall device design and materials utilized. The combination of high-k dielectrics and metal gates, while beneficial for leakage control and speed, must be carefully handled to ensure ideal transport conditions in nanosheet FETs.

5.3.7 NON-EQUILIBRIUM GREEN'S FUNCTION (NEGF) APPROACH

The non-equilibrium Green's function (NEGF) technique [36,37] offers a rigorous quantum mechanical framework for studying transport in nanosheet FETs, especially at the nanometer scale. This formalism incorporates the effects of quantum confinement and scattering processes, resulting in a full description of charge transport in nanoscale devices. The NEGF approach accurately predicts how carriers flow through a transistor in realistic operating settings, when both ballistic and diffusive transport can coexist.

The NEGF model represents electron transport as a non-equilibrium process, taking into consideration scattering mechanisms and device boundaries. This is critical for understanding the transport behavior of nanosheet FETs, which operate at high bias levels and short channel lengths. Researchers can use NEGF-based simulations to investigate the transport properties of nanosheet FETs in response to changing variables such as bias voltage, temperature, and device geometry, providing deeper insights into performance limits and potential optimizations for next-generation transistor technologies.

5.3.8 THERMAL EFFECTS ON TRANSPORT MECHANISM

Thermal effects [38–41] have a substantial impact on the transport mechanism in nanosheet FETs, especially as device scaling improves power density. As temperatures rise, phonon scattering increases, resulting in phonon-limited transport. This scattering disrupts the smooth flow of electrons, lowering ballistic transport and increasing channel resistance. High temperatures degrade ballistic transport, resulting in lower performance parameters such as drive current and switching speed. Effective thermal management measures, such as improved heat dissipation techniques, are critical for preserving nanosheet FET performance, particularly in high-power or high-frequency applications where overheating can compound the thermal effects. Proper thermal design ensures that the transistor continues to function efficiently despite temperature-induced transport constraints.

5.4 MODELING OF NANOSHEET FETs USING BALLISTIC TRANSPORT

Modeling nanosheet FETs using ballistic transport principles leads to a better understanding of charge carrier behavior in ultra-scaled devices [28–30]. At the nanoscale, standard drift-diffusion models fail to represent the intricacies of charge transport. Instead, ballistic transport models, which allow for little carrier scattering, provide a more accurate framework for estimating nanosheet transistor performance. This section describes the theoretical and computational methods used to investigate ballistic transport in nanosheet FETs, including the Landauer technique and the NEGF formalism.

5.4.1 Importance of Ballistic Transport in Nanosheet FETs

As electronics get smaller, ballistic transport becomes more important. Ballistic transport occurs when electrons flow through a channel with little to no scattering, as opposed to diffusive transport in larger devices. The ballistic regime is especially significant in nanosheet FETs, where channel lengths are frequently less than the electron mean free path.

Ballistic versus Diffusive Transport: In classic metal-oxide-semiconductor field-effect transistors (MOSFETs) with larger channels, electrons scatter often, resulting in diffusive transport. Because of the low channel length of nanosheet FETs, scattering events are reduced, and electrons move ballistically along the channel.

Performance Metrics: Ballistic transport models can help estimate critical device characteristics including as on-state current, threshold voltage, subthreshold slope, and drain current. These models also shed light on the restrictions imposed by quantum processes at nanoscale levels.

5.4.2 Landauer Approach to Ballistic Transport

The Landauer model is commonly used to describe ballistic transport in nanoelectronic devices, such as nanosheet FETs. This method treats the device channel as a quantum conductor, focusing on electron transmission probability from source to drain.

Transmission Probability: In the Landauer model, the current through the nanosheet FET is proportional to the probability that an electron will successfully transmit through the channel without scattering. This is expressed through the Landauer formula:

$$I = \frac{2q}{h}\int_{E_S}^{E_D} T(E)M(E)f_S(E) - f_D(E)\,dE \tag{5.2}$$

where E_S and E_D represent the energy at the source and drain terminals, respectively.

Quantum Conductance: The model also introduces the concept of quantized conductance, where the conductance of a ballistic channel is described by the quantum of conductance. The total conductance of the nanosheet FET depends on the number of available conduction channels and their transmission probabilities.

5.4.3 KEY ASSUMPTIONS IN BALLISTIC TRANSPORT MODELS

Several significant assumptions are used in ballistic transport models for nanosheet FETs to simplify the study while still capturing the fundamental physics of electron transport. One basic assumption is that scattering events, such as those induced by phonons, impurities, or defects, are considered insignificant, allowing electrons to flow ballistically from source to drain without interruption. This assumes little energy loss and resistive dissipation during transportation.

The potential barriers within the channel, as well as the nanosheet material's band structure, determine electron transmission probability. This includes considering the electron wavelength and its interaction with the material's shape. Furthermore, quantum confinement alters the energy band structure due to the nanosheet's narrow dimensions, influencing how carriers flow along the channel. These simplified assumptions make it easier to study and predict the behavior of nanosheet FETs under ballistic transport conditions, albeit some scattering and resistive effects may still occur.

5.4.4 NON-EQUILIBRIUM GREEN'S FUNCTION (NEGF) FORMALISM

For a more rigorous quantum mechanical treatment, the NEGF formalism is used to explain ballistic transport in nanosheet FETs. The NEGF framework provides a thorough explanation of carrier dynamics, taking into account both quantum confinement and scattering.

NEGF Equations: The NEGF formalism is based on solving a set of coupled equations for the Green's function and the self-energy of the system. These equations describe the probability amplitudes of electrons traveling through the channel, incorporating the effects of both ballistic transport and scattering. The key NEGF equations are:

$$G(E) = \left(E - H - \epsilon_S - \epsilon_D\right)^{-1} \tag{5.3}$$

where $G(E)$ is Green's function; E is the electron energy; H is the Hamiltonian of the system; and ϵ_S and ϵ_D are the self-energy terms for the source and drain contacts, respectively.

The Quantum Transport Model: NEGF provides a thorough representation of electron transport through the nanosheet FET. The formalism allows for the incorporation of scattering mechanisms (such as phonons and defects), making it a more accurate model for real-world devices than the simpler Landauer method.

Self-Consistent Solution: The NEGF equations must be solved using the Poisson equation, which describes the electrostatic potential in the device. This connection guarantees that the transport characteristics are estimated accurately, taking into account the gate voltage and any external biases.

5.4.5 BALLISTIC TRANSPORT IN MULTIGATE NANOSHEET FETs

The GAA architecture greatly improves ballistic transport conditions in multigate nanosheet FETs. The GAA structure enables the gate to entirely cover the channel, resulting in improved electrostatic control. This precise control improves carrier confinement by guaranteeing that electrons or holes travel in a more direct and regulated path from the source to the drain, limiting the possibility of scattering and short-channel effects. This arrangement improves ballistic transport because the confined carriers suffer fewer interruptions, making it easier for them to maintain high speeds across the channel length. When comparing ballistic and diffusive transport in GAA nanosheet FETs, the multigate structure helps to maintain ballistic transport over longer channels than standard MOSFETs or FinFETs. This results in a larger on-state current and faster switching speeds, which are critical for high-performance applications.

5.4.6 MATHEMATICAL MODELING OF BALLISTIC TRANSPORT

The mathematical explanation of ballistic transport in nanosheet FETs includes solving both the Schrödinger equation and the Poisson equation. These equations govern the quantum wavefunctions of electrons and the electrostatic potential.

Schrödinger Equation: The Schrödinger equation is used to calculate the energy states and the wavefunctions of the electrons in the nanosheet channel. These wavefunctions are crucial for determining the transmission probability of carriers in the ballistic regime.

$$H\psi = E\psi$$

where H is the Hamiltonian, Ψ is the wavefunction, and E is the energy eigenvalue.

Poisson Equation: The Poisson equation is used to calculate the electrostatic potential in the device. This potential influences the energy barriers that electrons must overcome to move from source to drain.

$$\frac{\partial^2\varphi}{\partial x^2} + \frac{\partial^2\varphi}{\partial y^2} = \frac{q}{\varepsilon} n(x, y) \tag{5.4}$$

where φ is the electrostatic potential, ε is the dielectric constant of the material, and n is carrier density in the channel.

Self-Consistent Solution: To precisely represent the charge distribution and potential profile in the nanosheet FET, the Schrödinger and Poisson equations must be solved in a consistent manner. This repeated procedure guarantees that electrostatic effects are appropriately represented in the transport model.

5.4.7 Impact of Material Properties on Ballistic Transport

The material properties of nanosheet FETs have a significant impact on the amount of ballistic transport within the device. The effective mass of charge carriers, the gate insulator's dielectric constant, and the channel material's bandgap all have a significant impact.

The effective mass of the carriers determines how quickly electrons or holes can pass across the channel. Materials with low effective mass allow carriers to move more freely, which promotes ballistic transport. III–V semiconductors, such as InGaAs, have a substantially lower effective mass than silicon, making them ideal for ballistic nanosheet FETs because they allow electrons to flow more quickly with less scattering.

The use of high-k dielectrics in the gate stack, such as hafnium oxide (HfO_2), enhances electrostatic control by lowering gate leakage, but it also changes the electric field distribution within the channel. This can alter electron transmission probability in the ballistic regime, necessitating careful optimization to strike a balance between control and ballistic performance.

Additionally, the bandgap of the channel material influences carrier injection from the source to the channel. A tight bandgap improves carrier injection but raises the possibility of leakage currents, necessitating materials with the appropriate balance for ballistic transport to prevail.

In conclusion, knowing and improving these material properties are critical for modeling nanosheet FETs with ballistic transport principles. Techniques such as the Landauer technique and the NEGF formalism enable precise simulations of nanosheet FET performance, providing important insights for future semiconductor device design.

5.5 RESULT ANALYSIS AND DISCUSSIONS

5.5.1 Performance Metrics of Nanosheet FETs

The major purpose of the analysis is to assess nanosheet FET performance measures, such as drain current, subthreshold slope, threshold voltage, and transconductance, in the ballistic transport regime. These parameters are crucial for defining the efficacy and scalability of nanosheet FETs in future semiconductor technologies.

5.5.1.1 Drain Current (I_{ds})

Figure 5.4 represents the drain current versus gate voltage characteristics for a semiconductor device with different channel lengths ($L = 12$, 20, 30, and 40 nm). The plot

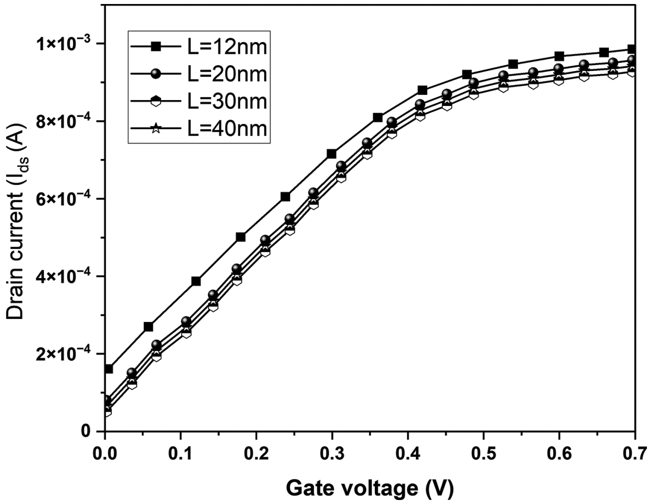

FIGURE 5.4 The drain current versus gate voltage characteristics with different channel lengths.

shows the relationship between the applied gate voltage and the corresponding drain current for these four channel lengths, indicating the device's behavior under various scaling conditions. As the gate voltage increases from 0 to 0.7 V, the drain current increases linearly for each channel length, displaying the device's threshold voltage and current saturation behavior. The trend reveals that shorter channel lengths (L = 12 nm) exhibit higher drain current values compared to longer channel lengths (L = 40 nm), due to reduced resistance and enhanced carrier mobility in shorter devices. The plot also indicates that as the channel length increases, the drain current decreases for the same gate voltage, demonstrating the impact of channel length on the device's electrical performance. The current difference between various channel lengths becomes more pronounced at higher gate voltages, highlighting the importance of channel length scaling for optimizing the device's current drive capability.

5.5.1.2 Threshold Voltage (V_{th})

Figure 5.5 illustrates the relationship between the threshold voltage (V_{th}) and the channel length of a nanosheet FET at two different drain–source voltages (V_{DS}). The x-axis represents the channel length (in nanometers), ranging from 10 to 50 nm, while the y-axis represents the threshold voltage (in volts), ranging from 0.28 to 0.34 V. Orange Squares (Curve for V_{DS} = 0.7 V): This curve shows an increasing trend in threshold voltage as the channel length increases up to approximately 30 nm, after which it plateaus. Circles (Curve for V_{DS} = 50 mV): This curve exhibits a peak in threshold voltage at around 20 nm, followed by a decrease and then leveling off. As the channel length decreases, short-channel effects become more pronounced. These effects include DIBL and threshold voltage roll-off, which can significantly impact the device's electrical characteristics. For the curve at V_{DS} = 0.7 V, the increasing trend in V_{th} with channel length suggests that short-channel effects are mitigated as

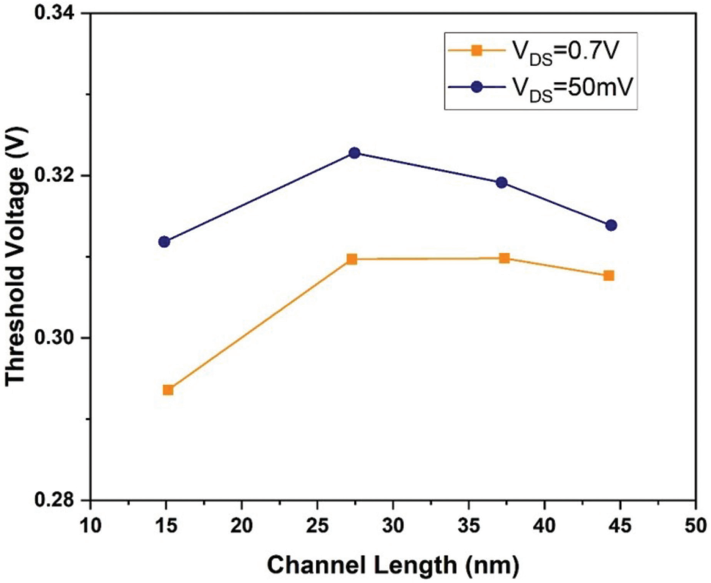

FIGURE 5.5 The threshold voltage versus the channel length of a nanosheet FET at two different drain–source voltages.

the channel length increases, leading to a more stable threshold voltage. The plateau beyond 30 nm indicates that the device is less susceptible to short channel effects at longer channel lengths. DIBL is more pronounced at higher drain–source voltages. It causes a reduction in the threshold voltage as the drain voltage increases, due to the lowering of the potential barrier at the drain end of the channel. The curve for $V_{DS} = 50\,\text{mV}$ shows a peak at around 20 nm, indicating an optimal channel length where the threshold voltage is maximized. Beyond this point, the threshold voltage decreases due to the onset of DIBL and other short-channel effects.

5.5.1.3 Subthreshold Swing (SS)

Figure 5.6 presents the subthreshold swing (SS) as a function of the drain current for both pFET (black squares) and nFET (red circles) devices. The subthreshold swing (measured in mV/decade) is a key parameter in characterizing the switching behavior of transistors, particularly in the subthreshold region, where the transistor operates below the threshold voltage. In the plot, both pFET and nFET devices exhibit a similar trend, where the subthreshold swing remains low at lower drain current values and increases significantly as the current rises. The graph covers a range of drain currents from 10^{-8} A/µm to 10^{-7} A/µm, indicating that the SS for both devices is minimal in the lower current regime and rapidly increases as the drain current approaches higher values. For the pFET, the SS starts around 50 mV/dec at low I_D, gradually increasing with current, showing a steeper rise near $I_D = 9 \times 10^{-8}$ A/µm. Similarly, the nFET follows the same trend but has a slightly lower subthreshold swing in the higher current range. This behavior suggests that both transistors experience degradation in

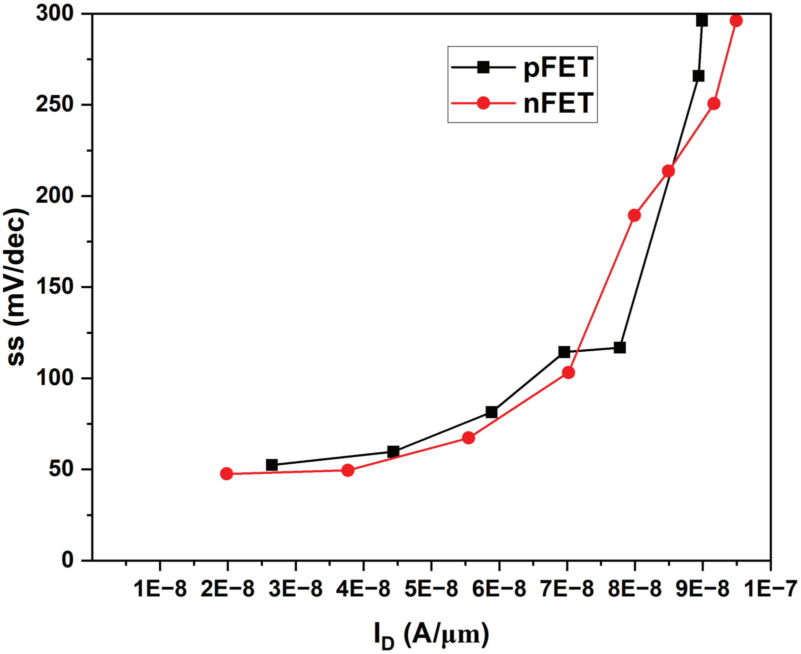

FIGURE 5.6 The subthreshold swing (SS) as a function of the drain current.

switching efficiency as the drain current increases, though pFETs and nFETs exhibit comparable performance in terms of subthreshold swing across the current range, with slight differences at higher I_D. This analysis is critical in optimizing transistor designs for energy-efficient switching and low-power applications.

5.5.1.4 Transconductance (g_m)

Figure 5.7 presents the transconductance (g_m) characteristics of a nanosheet FET as a function of gate voltage (V_G). Transconductance is a critical parameter in FETs, representing the rate of change of the drain current (I_D) with respect to the gate voltage (V_G). This x-axis represents the voltage applied to the gate terminal of the FET. The y-axis indicates the transconductance value. There are two distinct curves in the graph: Black Squares (Curve for $V_{DS} = 700\,mV$): This curve shows a monotonic increase in transconductance as the gate voltage increases. The transconductance starts from a low value at $V_G = 0$ and rises steadily, indicating that the device is in the saturation region where the drain current increases with gate voltage. Red Circles (Curve for $V_{DS} = 50\,mV$): This curve exhibits a peak in transconductance at around $V_G = 0.2\,V$. After reaching the peak, the transconductance decreases, suggesting that the device transitions from the linear region to the saturation region as the gate voltage increases. High V_{DS} (700 mV): The steady increase in g_m with V_G indicates strong channel formation and enhanced carrier mobility, leading to higher drain current. This behavior is typical in the saturation region where the FET operates as a constant current source. Low V_{DS} (50 mV): The peak in gm at a lower gate voltage suggests

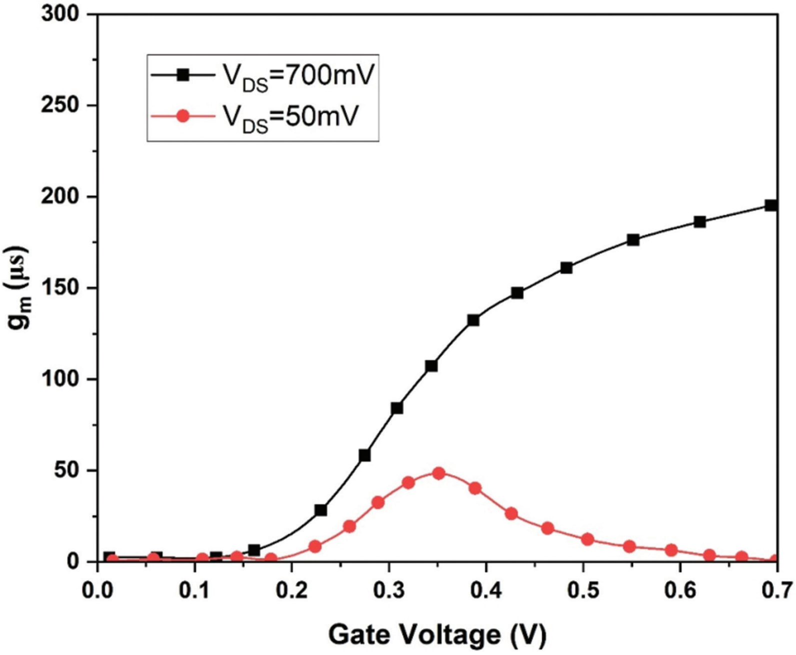

FIGURE 5.7 The transconductance (g_m) characteristics of a nanosheet FET as a function of gate voltage (V_G).

that the device initially operates in the linear region, where the drain current is proportional to both V_G and V_{DS}. As V_G increases further, the device enters the saturation region, causing g_m to decrease.

5.5.1.5 Non-Ballistic and Ballistic Transport

Figure 5.8 shows the non-ballistic and ballistic subthreshold current for varying channel length for various oxide thickness with metal work function value considered as 4.62 eV [28]. Figure 5.9 shows the non-ballistic and ballistic subthreshold current for varying channel length for various oxide thickness with metal work functions value considered as 4.42 and 4.62 eV [28].

5.5.2 DISCUSSION OF KEY FINDINGS

Benefits of Ballistic Transport: The analysis will highlight the advantages of using nanosheet FETs in the ballistic domain, such as increased current drive, better subthreshold slope, and enhanced energy efficiency. These benefits make ballistic transport models critical for future device scalability and performance optimization.

Challenges and Limitations: While ballistic transport has many advantages, issues like scattering and self-heating must be addressed. The shortcomings of present models in adequately capturing these impacts will be examined,

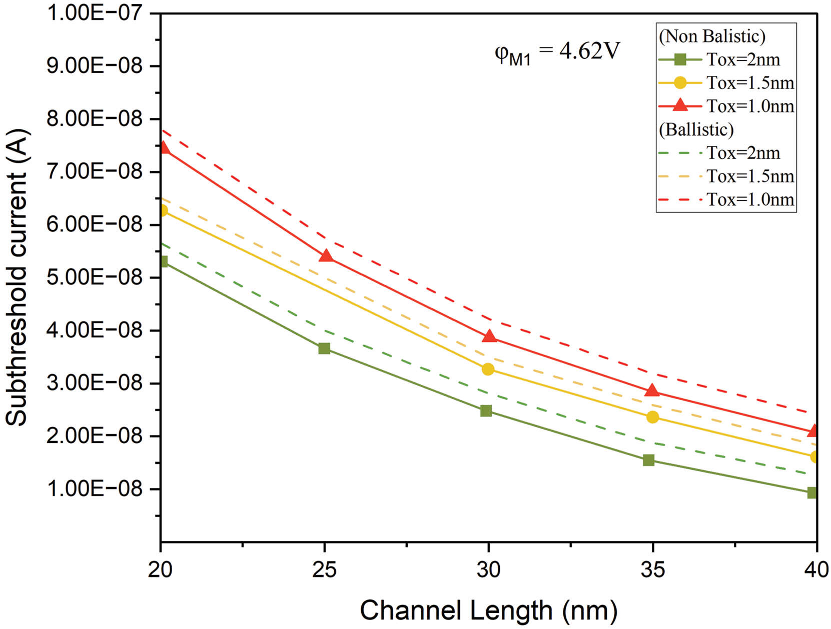

FIGURE 5.8 The non-ballistic and ballistic subthreshold current for varying channel length for various oxide thickness.

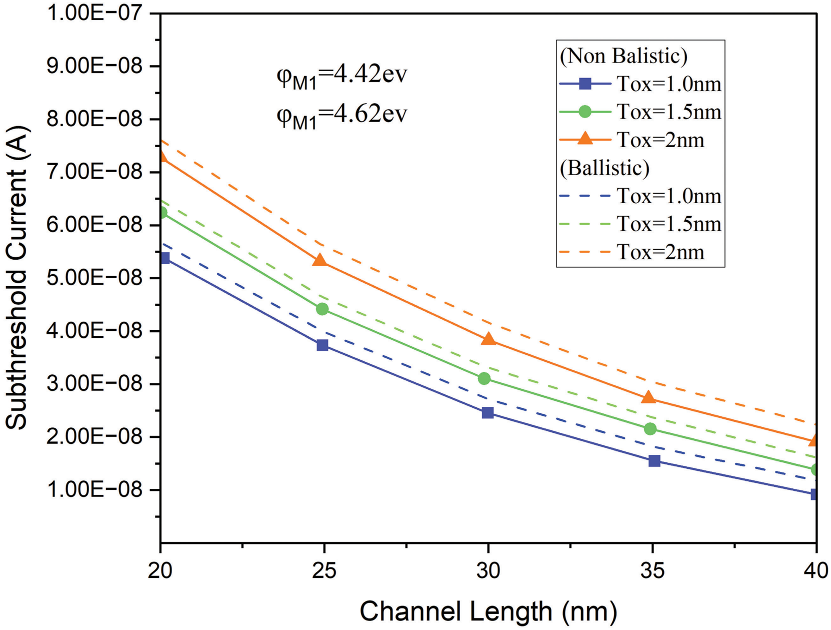

FIGURE 5.9 The non-ballistic and ballistic subthreshold current for varying channel length for various oxide thickness.

as well as prospective advances in modeling tools and experimental procedures to better account for these variables.

Path Forward: Finally, the presentation will outline the future research directions required to address the remaining issues in nanosheet FETs, particularly the integration of quasi-ballistic and quantum transport models. Emerging advances in material engineering, device architecture, and machine learning-based modeling will be emphasized as promising areas for further investigation.

5.6 FUTURE ASPECTS OF TRANSPORT MECHANISM

The fast growth of nanoscale transistor technology, particularly nanosheet FETs, is opening up new horizons in the transport mechanisms that determine device performance. As transistors are reduced to atomic size, traditional transport models may no longer represent the complexities of carrier behavior in these ultra-scaled regimes. This section investigates future research objectives and difficulties related to transport mechanisms in nanosheet FETs, with a particular emphasis on quantum transport, material innovation, and innovative topologies.

5.6.1 Exploring Quantum Transport beyond Ballistic Regimes

While ballistic transport models have given us valuable insights into nanosheet FET operation, the future rests in investigating quantum transport mechanisms that go beyond conventional ballistic models. As devices shrink further, the electron's wave-like nature becomes more apparent, and quantum coherence and tunneling take precedence.

Quantum Coherence: At extremely short channel lengths, quantum coherence between electrons begins to influence how carriers move along the channel. This could result in wavefunction interference, necessitating the development of new quantum mechanical models capable of accurately predicting current flow and device performance. Research into how these interference patterns affect transport qualities is an essential future focus.

Tunneling Effects: As channel lengths approach the de Broglie wavelength of electrons, tunneling through potential barriers increases significantly. Tunneling FETs (TFETs) may become a viable alternative to regular MOSFETs, as tunneling current can be used to improve switching behavior and energy efficiency. The transport process in tunnel-based nanosheet FETs may give ultralow power solutions, but comprehending tunneling in these ultra-scaled devices remains a challenge.

5.6.2 Hybrid Transport Mechanisms: Quasi-Ballistic to Fully Quantum

The shift from ballistic to fully quantum transport reflects a hybrid regime known as quasi-ballistic transport, in which scattering re-emerges in some regions of the channel. The future of nanosheet FETs is to understand and create devices that take use of this quasi-ballistic transport for improved performance.

Quasi-Ballistic Transport Models: Hybrid models that account for both ballistic and scattering effects will be required to accurately anticipate the behavior of future nanosheet FETs. These models will need to include electron-phonon interactions, impurity scattering, and surface roughness scattering, all of which will become increasingly important as device dimensions decrease.

Self-Healing Transport: Self-healing transport mechanisms are a new area of research in which the transport properties of nanoscale devices are tailored to reduce the impacts of scattering. Researchers are experimenting with creating defect-tolerant materials or using adaptive biasing systems to preserve ballistic or quasi-ballistic transport in the presence of defects.

5.6.3 IMPACT OF NEW MATERIALS ON TRANSPORT MECHANISMS

One of the most interesting future avenues in transport mechanisms is the discovery of novel materials with unique features that have the potential to transform carrier transportation. Two-dimensional (2D) materials, topological insulators, and carbon-based materials such as graphene and carbon nanotubes (CNTs) are particularly well studied for enhancing carrier mobility and minimizing scattering.

2D Materials: Transition metal dichalcogenides (TMDs) like MoS_2 and WS_2 are ideal for nanosheet FETs due to their high mobility, mechanical flexibility, and atomically thin channel lengths. Because of their distinct band structures, these materials have the potential to push the limits of quantum transport by allowing for practically scattering-free carrier travel.

Topological Insulators: Topological insulators have extremely conductive surface states that are shielded by time-reversal symmetry, allowing for dissipationless transport across the surface. Incorporating topological insulators into nanosheet FETs may enable new types of transport mechanisms in which surface currents dominate, resulting in extremely low-power operation.

Graphene and Carbon Nanotubes: Graphene's fast electron mobility and zero bandgap structure provide novel prospects for high-speed nanosheet FETs. Similarly, CNTs are being studied for their one-dimensional transport capabilities, which reduce scattering and improve ballistic transport. In the future, graphene and CNT-based FETs may be specifically built for ultra-fast, low-power applications.

5.6.4 NOVEL DEVICE ARCHITECTURES AND TRANSPORT MECHANISMS

Novel device architectures that differ from classic MOSFET designs will also have an impact on the future of transport systems. 3D stacked FETs, vertical nanosheet transistors, and neuromorphic transistors are emerging as promising answers to present technical limits. These structures present additional challenges for understanding transport mechanisms, specifically how electric fields, quantum confinement, and surface states interact.

Vertical Nanosheet FETs: The development of vertical nanosheet transistors could have a substantial impact on ballistic and quantum transport. In these devices, electrons migrate vertically rather than laterally, altering the electrostatic potential profile and influencing carrier movement through the channel.

Stacked Nanosheet Architectures: 3D stacked FET topologies may bring new types of transport processes, with interlayer interaction between distinct nanosheets influencing electron mobility and subthreshold behavior. These layouts enable better device density, but they also present novel issues in temperature control and inter-sheet carrier transfer.

Neuromorphic and Bio-Inspired Devices: The future of electronics may include neuromorphic architectures that replicate brain function, necessitating a new knowledge of transport mechanisms in devices that blend electrical, ionic, and biological elements. Bio-inspired nanosheet FETs have the potential to enable new transport paradigms by merging classical, quantum, and biological transport mechanisms for novel computation and sensing applications.

5.6.5 TRANSPORT MECHANISM IN HIGH-TEMPERATURE AND HARSH ENVIRONMENTS

As nanosheet FETs are pushed into new applications such as automotive, space, and industrial environments, their ability to operate in severe situations will be determined by the transport mechanism's resilience to factors such as temperature, radiation, and mechanical stress.

High-Temperature Operation: At higher temperatures, phonon scattering becomes more noticeable, limiting carrier mobility and the efficacy of ballistic transport. The challenge for future nanosheet FETs is to create transport models that can forecast performance at high temperatures, as well as to build materials that reduce the impact of thermal scattering.

Radiation-Hardened Devices: In space applications, radiation-induced flaws might introduce traps and enhance scattering events, reducing transport. Future transport models must take radiation into consideration and aid in the construction of radiation-hardened nanosheet FETs that work well even when bombarded with high-energy particles.

5.6.6 INTEGRATION OF MACHINE LEARNING FOR PREDICTIVE MODELING

The increasing complexity of transport mechanisms in nanosheet FETs, along with the enormous parameter space involved in device design, renders traditional modeling methodologies ineffective. Machine learning (ML) and artificial intelligence (AI) are developing as strong technologies for predictive modeling and improvement of transportation systems.

- **Data-Driven Models**: By training ML algorithms on vast datasets of nanosheet FET simulations and experiments, researchers may create prediction models that accurately capture transport pathways without the need for time-consuming first-principles calculations.
- **Optimization of Transport Properties**: ML can also be used to optimize transport qualities by determining the optimal combinations of materials, geometries, and biasing conditions to maximize performance. This could result in the quick creation of new device architectures with improved transport capabilities.

To summarize, the future of transport processes in nanosheet FETs lies in the study of quantum effects, new materials, and novel topologies. As devices scale, ML for predictive modeling and optimization will become increasingly important in creating the next generation of nanosheet FETs for high-performance applications in electronics, computation, and sensing.

5.7 CONCLUSION

Nanosheet FETs are a promising improvement in transistor technology, providing superior electrostatic control and improved performance, particularly as devices are scaled down to the nanoscale regime. This book chapter investigated the transition from classical to quantum transport, focusing on ballistic transport models. Ballistic transport improves control over important parameters like drain current, threshold voltage, and subthreshold slope by reducing scattering and leveraging carriers' quantum nature.

The Landauer method and other quantum transport models give a solid foundation for understanding charge transport mechanisms in nanosheet FETs. Simulations and experimental data show that these models effectively predict the performance parameters of nanosheet FETs under a variety of situations. However, issues like scattering events, self-heating effects, and short-channel effects must be solved before widespread usage in advanced semiconductor applications.

Moving forward, breakthroughs in material engineering, device architecture, and thermal management will be critical in improving nanosheet FETs for future technological nodes. Nanosheet FETs, by continuing to bridge the gap between classical and quantum transport, have the potential to generate major advances in energy efficiency, switching speed, and device scaling, establishing them as a cornerstone of future electronics.

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6 Classical to Semiclassical Transport in Field Effect Transistors

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6.1 FUNDAMENTALS OF CHARGE TRANSPORT

6.1.1 BASIC CONCEPTS OF CHARGE TRANSPORT

In the classical era, understanding electron behavior in materials relied on classical physics principles. For instance, the free electron model depicted electrons as free agents darting about a material, blissfully ignoring the atomic lattice [1]. This model was akin to treating electrons as marbles rolling around in a box, helping us grasp concepts like electrical conductivity and other macroscopic properties. Building on this, Paul Drude's 1900 model applied classical physics to elucidate electrical and thermal conductivity by envisioning electrons as classical particles with an effective mass, offering valuable insights into material transport properties.

Then, in 1900, Max Planck introduced a revolutionary idea: thermal radiation is emitted in discrete packets of energy known as quanta [2]. Jump ahead to 1905, and Albert Einstein leveraged this concept to shed light on the photoelectric effect, suggesting that light behaves more like energetic particles than a smooth, undulating wave. This particle-like behavior also played a pivotal role in explaining the Compton effect. In 1924, Louis de Broglie brought a fresh perspective, proposing that if waves could act like particles, then particles should display wave-like properties [3]. The Heisenberg uncertainty principle, unveiled in 1927, took this idea further by stating that we can't precisely measure both the position and momentum of a tiny particle simultaneously [4]. Picture trying to pin down an electron's precise position in addition to momentum at the same instance—it's a quantum no-no! Similarly, measuring an electron's energy and the exact moment it has that energy is equally elusive. Rather than tracking electrons like a GPS, we use probability functions to estimate where they might be. It's more like predicting where your friend could be in a packed party rather than locating them with pinpoint accuracy. In 1926, Erwin Schrödinger introduced wave mechanics, blending Planck's quantum ideas with de Broglie's wave-particle duality [5]. His equation enabled the calculation of energy levels and wavefunctions of electrons in a crystal, crucial for deciphering band structures.

Carrier transport then ushered in band theory, describing how allowed and forbidden energy levels (bands and band gaps) emerge from the interactions of electrons

DOI: 10.1201/9781003543923-6

with periodic potential in crystal lattice. This theory helps us understand why materials behave as conductors, semiconductors, or insulators based on their electronic band structure. Felix Bloch contributed significantly to this area of physics by demonstrating that electron wavefunctions within a periodic potential can be expressed as a plane wave combined with a function exhibiting the same periodicity as the potential. This theorem was key to deriving the electronic band structure in solids. Essentially, this means that the wavefunctions can be expressed as a product of a function that varies with position and a complex exponential term, which captures the periodic nature of the potential. When two atoms are brought close together, their electron wavefunctions start to overlap, creating interactions between the electrons [6]. This overlap, or perturbation, results in the splitting of previously distinct quantized energy levels into two separate levels. This division complies with the Pauli exclusion principle, which dictates that two electrons cannot occupy the same quantum state simultaneously. To tackle Schrödinger's wave equation for a one-dimensional single-crystal lattice, we simplify our approach using a more manageable potential function. Kronig–Penney model captures the periodic potential of a single-crystal lattice [7]. To solve Schrödinger's wave equation effectively, we examine each region individually. Just like other quantum mechanical systems, the most fascinating results appear when energy of a particle is lower than the potential, indicating that the particle is trapped within the crystal. Even though electrons are confined in potential wells, they still have the chance to tunnel between these wells.

As the temperature rises above absolute zero, a number of electrons in the valence band may gain an adequate amount of thermal energy to break free from covalent bonds and move into the conduction band, keeping the semiconductor electrically neutral. This creates a situation where one empty state is filled while a new empty state is created—effectively mimicking the movement of a positive charge in the valence band. Remarkably, an electron near the upper edge of a permitted energy band exhibits behavior akin to having a negative mass, yet it continues to move in alignment with the direction of the applied electric field. To simplify things, we can model this behavior by considering particles in the band as having positive charge as well as positive effective mass, denoted as *hole*. This makes it easier to relate the complex quantum behavior of electrons to more intuitive, classical ideas of motion.

It is to be noted that when we deal with a large group of particles, instead of focusing on each individual particle, we are more interested in how the group behaves statistically as a whole. For instance, the electrical properties of materials aren't determined by the actions of single electrons but by the collective behavior of a large number of them. To understand how these particles distribute themselves among different energy levels, we use three main statistical laws. (a) *Maxwell–Boltzmann Distribution* [8]: The particles are treated as distinguishable, no restriction on how many particles can occupy each energy state, e.g., gas molecules at low pressure. (b) *Bose–Einstein Distribution* [9]: The particles are indistinguishable, no limit to the number of particles that can occupy each energy level, e.g., photons. (c) *Fermi–Dirac Distribution*: The entities are indistinguishable from one another, yet a single entity can occupy a given quantum state at a time, assuming that the particles don't interact with each other, e.g., electrons and holes in a crystal [10].

6.1.2 SCATTERING MECHANISMS

In classical physics, scattering is all about how particles or waves get redirected when they interact with other particles, obstacles, or fields. Imagine a ball bouncing off a wall—scattering is essentially that redirection. Classical theories explain these interactions through Newtonian mechanics and Maxwell's equations (so, no quantum mechanics here yet!). The process of scattering focuses on how particles change their paths, and key principles like energy and momentum conservation are at play.

In semiconductors, two primary scattering mechanisms, namely phonon (lattice) scattering and ionized impurity scattering, play a big role in impacting carrier mobility [11]:

6.1.2.1 Phonon (Lattice) Scattering

Phonon scattering refers to the interaction of charge carriers (e.g., electrons, holes) with vibrations in the crystal lattice of a semiconductor. In a crystal lattice, atoms are not stationary but vibrate around their equilibrium positions [12]. These vibrations are quantized as phonons, which represent energy packets of lattice vibrations. When charge carriers move through the lattice, they scatter off these phonons. Scattering alters the carriers' momentum and energy, leading to a decrease in their ability to move freely.

Phonon scattering is temperature-dependent [13]. These vibrations increase with temperature, leading to more phonons. At higher temperatures, more phonons are present, leading to increased scattering and decreased carrier mobility. This is why mobility in semiconductors tends to decrease with increasing temperature. There are again two types of phonon scattering, namely:

i. **Acoustic Phonon Scattering**: Occurs owing to the interaction of carriers with low-energy, long-wavelength vibrations (acoustic phonons). It dominates at lower temperatures. The mobility decreases as the temperature increases, showing an inverse relationship [14].
ii. **Optical Phonon Scattering**: Involves higher-energy phonons (optical phonons) and becomes more significant at higher temperatures. Optical phonon scattering occurs when carriers exchange energy with phonons, typically leading to larger energy losses compared to acoustic phonon scattering [15].

6.1.2.2 Ionized Impurity Scattering

Ionized impurity scattering occurs when charge carriers interact with electrically charged impurities within the semiconductor material [16]. These impurities can be dopants that have been added to alter the conductivity of the material, or they can be unintentional defects as they introduce either free electrons (n-type) or holes (p-type), are ionized, and create local electric fields that interact with moving carriers. When a carrier moves near an impurity, the Coulomb force from the impurity alters its path, leading to scattering. Unlike phonon scattering, ionized impurity scattering depends more on the Coulomb interaction between carriers and impurities and is less affected by temperature changes.

6.1.3 CARRIER MOBILITY, DRIFT, AND DIFFUSION

6.1.3.1 Mobility

Imagine applying an electric field (F) to a semiconductor. This field exercises a force on carriers, causing them to accelerate and move. Now, the key is that for this movement to happen, there must be accessible energy states in conduction and valence bands, like rungs on a ladder for them to climb.

As the hole in the crystal accelerates under the control of the electric field, its velocity boosts. But here's the catch: every so often, it will collide with atoms in the crystal, which causes it to lose most, if not all, of its energy. The hole then starts accelerating again, only to be interrupted by another scattering event. This process repeats itself over and over.

The time between collisions in a semiconductor is called the "mean free time (τ_p, τ_n)" [17]. During this interval, charged particles such as electrons or holes accelerate due to the applied electric field, gaining energy. Once a collision occurs, they lose most of their energy, and the cycle of acceleration begins again.

In light of above, the mean peak velocity (v_p, v_n) defined just before a collision is [18]

$$v_p = \left[\frac{q\tau_p}{m^*_p}\right]F \tag{6.1}$$

$$v_n = -\left[\frac{q\tau_n}{m^*_n}\right]F \tag{6.2}$$

p and n denoting holes and electrons in every notation in this chapter.

Can be put as written in equations. 6.3 and 6.4

$$v_p = \mu_p F \tag{6.3}$$

$$v_n = -\mu_n F \tag{6.4}$$

where q is the electron/hole charge, m^*_p, m^*_n are respective effective mass of hole and electron, μ_p and μ_n are the proportionality factor defined as "hole and electron mobility," respectively.

In relation with the scatterings defined in the previous section, the scattering rate due to phonons (6.1.2.1.1) can be obtained from Fermi's golden rule and is proportional to the number of available phonons. The mobility (μ_{phonon}), obtained if only phonon scattering is assumed, decreases with temperature (T), as phonon population increases with temperature, contributing to reduced mobility. μ_{phonon} can be approximated by

$$\mu_{\text{phonon}} \propto T^{-3/2} \tag{6.5}$$

On the other hand, the mobility limited by ionized impurity scattering (6.1.2.2), μ_{impurity}, is often described by Brooks–Herring or Conwell–Weisskopf model, and it increases with temperature (T) and can be approximated by [19].

$$\mu_{\text{impurity}} \propto \frac{T^{3/2}}{N_{\text{impurity}}} \tag{6.6}$$

where N_{impurity} is the impurity concentration. At lower temperatures, impurity scattering dominates since phonon scattering diminishes. The extent of ionized impurity scattering can be reduced by screening, where other carriers in the semiconductor shield the moving carriers from the full impact of the impurity's Coulombic field. The Debye screening length quantifies how effectively carriers are screened in the material. Higher carrier concentrations reduce the scattering effect by screening the impurity's electric field.

If these two scattering processes are considered independent, then the likelihood of a scattering event happening within a small time frame is simply the sum of the probabilities for each individual process. This additive nature also applies to the overall mobility, where the net mobility (μ_{net}) is derived from the combination of both scattering mechanisms [20–23]:

$$\frac{1}{\mu_{\text{net}}} = \frac{1}{\mu_{\text{phonon}}} + \frac{1}{\mu_{\text{impurity}}} \tag{6.7}$$

6.1.3.2 Diffusion

Imagine particles moving from an area where they're crowded (high concentration) to a place where there's more space (low concentration). Now, if those gas molecules are charged, this movement creates what we call a diffusion current [21] (Figure 6.1).

For our calculations, we'll assume that the temperature is consistent throughout, meaning the average speed of the electrons doesn't change based on their position (x). To find the current, we'll focus on how many electrons are flowing across a specific area at a given time, particularly at the point. The net rate of electrons (R_n) and holes (R_p) flowing in a set direction is obtained by Taylor series expansion and is given by

$$R_p = -v_p l_p \frac{dN_p}{dx} \tag{6.8}$$

$$R_n = -v_n l_n \frac{dN_n}{dx} \tag{6.9}$$

where l_p and l_n are the distances traveled by hole and electron before collisions with velocity v_p and v_n, dN_p/dx and dN_n/dx being the density gradients (DGs) over distance, respectively.

So, the diffusion current is [24]

$$J_p^{\text{diff}} = qR_p = -qv_p l_p \frac{dN_p}{dx} = -qD_p \frac{dN_p}{dx} \tag{6.10}$$

$$J_n^{\text{diff}} = -qR_n = qv_n l_n \frac{dN_n}{dx} = qD_n \frac{dN_n}{dx} \tag{6.11}$$

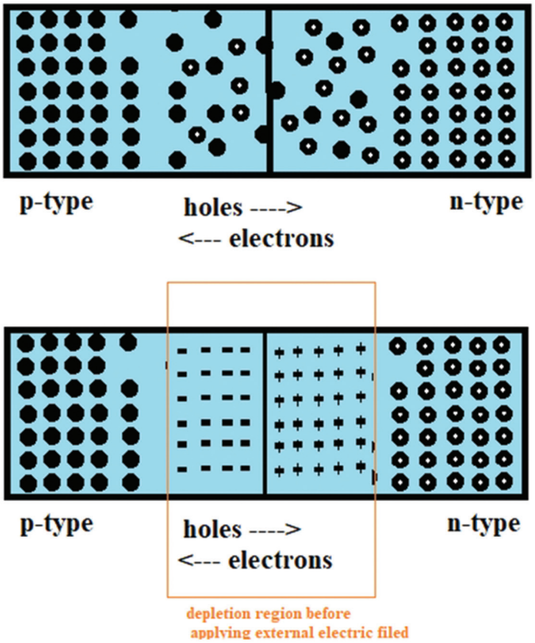

FIGURE 6.1 Diffusion process and creation of space charge region.

D_p and D_n are the hole and electron diffusion coefficients, respectively, both positive, having the unit of cm^2/s.

6.1.3.3 Drift

Through all these interactions, the hole settles into an average drift velocity. What's interesting is that at low electric fields, this drift velocity is directly proportional to the electric field—meaning the stronger the field, the faster the particle moves [20] (Figure 6.2).

Now, for electrons, it's a similar story. The electron's average drift velocity also scales with the electric field for small fields. But since electrons are negatively charged, their motion is in the reverse direction of the electric field.

The drift current density for hole and electron ($J_p{}^{\text{drift}}$ and $J_n{}^{\text{drift}}$) at volume charge density (N_p and N_n) now can be expressed as [21]

$$J_p{}^{\text{drift}} = qN_p v_p = qN_p \mu_p F \tag{6.12}$$

$$J_n{}^{\text{drift}} = -qN_n v_n = qN_n \mu_n F \tag{6.13}$$

The net drift current density (J) is

$$J = J_p{}^{\text{drift}} + J_n{}^{\text{drift}} = qN_p \mu_p F + qN_n \mu_n F = \sigma F \tag{6.14}$$

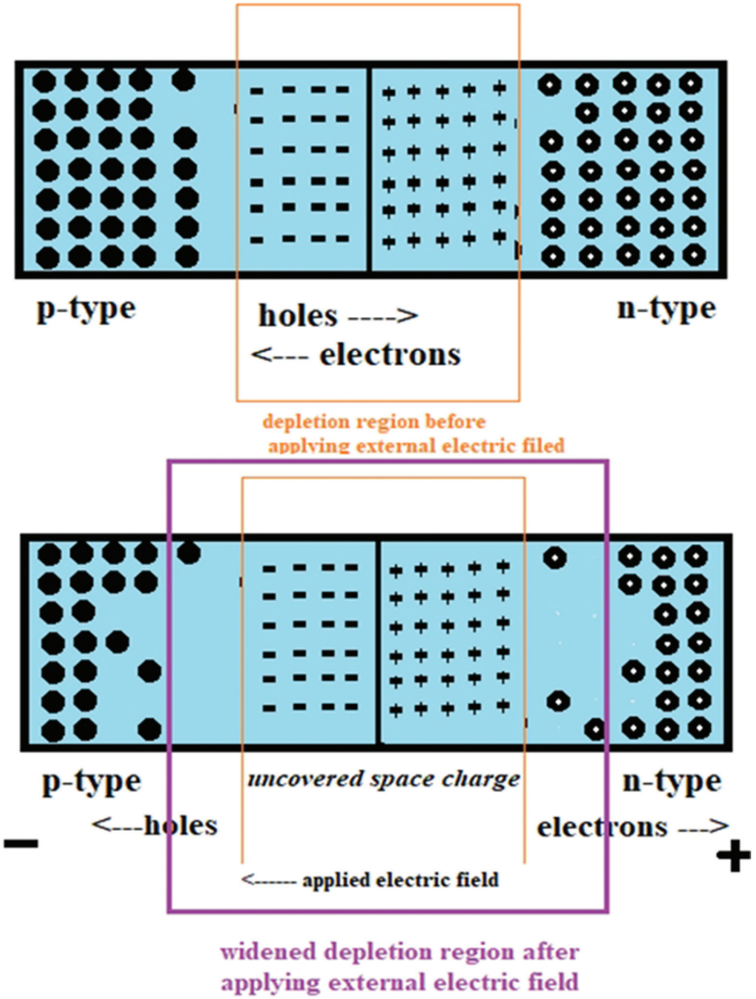
p-type
holes ---->
<--- electrons
n-type
depletion region before
applying external electric filed
p-type
uncovered space charge
n-type
<---holes
electrons --->
−
+
<------ applied electric field
widened depletion region after
applying external electric field

FIGURE 6.2 Drift process and widening of space charge region.

σ being the conductivity having unit $(\Omega \text{ cm})^{-1}$, and its reciprocal is the resistivity.

The *conductivity and resistivity* of an extrinsic semiconductor are mainly determined by the *properties of the majority carriers and temperature* [22]. At moderate temperatures (the extrinsic range), the semiconductor's dopant atoms are entirely ionized, meaning the number of majority carriers (electrons or holes) stays fairly constant. However, the mobility of these carriers, which influences how easily they move through the material, relies on temperature, causing changes in overall conductivity.

As temperature rises, the inherent carrier concentration (carriers generated thermally) rises and begins to dominate the semiconductor's behavior, impacting both the carrier concentration and the conductivity. In contrast, at low temperatures, a process called freeze-out occurs, where the carriers become trapped, reducing both the electron concentration and the material's conductivity.

Let's explore the concept of *velocity saturation* [23]. Earlier, we assumed that the mobility of charge carriers remains constant and that drift velocity is a linear function of electric field. In simpler terms, as you increase the electric field, the drift velocity of the electrons as well as holes increases proportionally—up to a certain point. Now, in reality, things get more interesting at high electric fields. The total velocity of a particle combines both the random thermal velocity and the drift velocity. At small electric fields, the relationship between drift velocity and the electric field is linear. However, as the electric field becomes stronger, this linear relationship breaks down, and the drift velocity approaches a saturation velocity.

An electron's movement in a lattice is quite different from how it behaves in free space. Here, it's not just the external forces at play but also internal forces within the crystal—like the tug-of-war between positively charged ions and electrons—that influence its motion. Here comes the concept of the *effective mass* (m^*), which accounts not only for the electron's actual mass but also the impact of these internal forces.

The energy-k diagram essentially captures both internal and external forces acting on the electron within a crystal. This allows us to link the effective mass of the electron to the contour of the E-versus-k curve (will be discussed in detail in subsequent sections):

$$E = \frac{p^2}{2m^*} = \frac{\hbar^2 k^2}{2m^*} \tag{6.15}$$

For an electron, the E-versus-k curve typically takes on a parabolic shape, reflecting the relationship between energy and momentum in the crystal (Figure 6.3). The second-order derivative of E with respect to k gives us valuable insight into the particle's mass, as it is inversely proportional to it. For a free electron, this relationship is straightforward—the mass is constant and positive, meaning the E-versus-k curve is parabolic with a consistent curvature. In the case of free electrons, there are no complicating internal forces, so the effective mass simply equals the electron's actual mass, making the motion predictable and regular.

When electric field is functional to a free electron at the bottom of an allowed energy band—often approximated as a parabola—the electron's energy alters, and the base of the band shifts away from its ideal parabolic shape. This shift is captured by the concept of effective mass, a crucial parameter that bridges the gap between quantum mechanics and classical physics. Essentially, the effective mass adjusts the classical force equations to account for quantum mechanical effects and internal forces within the crystal. In many cases, we can take care of an electron at the underneath of the conduction band like a classical particle, using Newtonian mechanics, as long as we factor in the electron's effective mass to account for its more complex behavior. So, the effective mass helps explain how an electron "feels" as it moves through the lattice, factoring in all the bumps and nudges along the way.

As the electric field increases, it gives electrons more energy, and eventually, they get scattered into higher energy states, known as upper valleys in the conduction

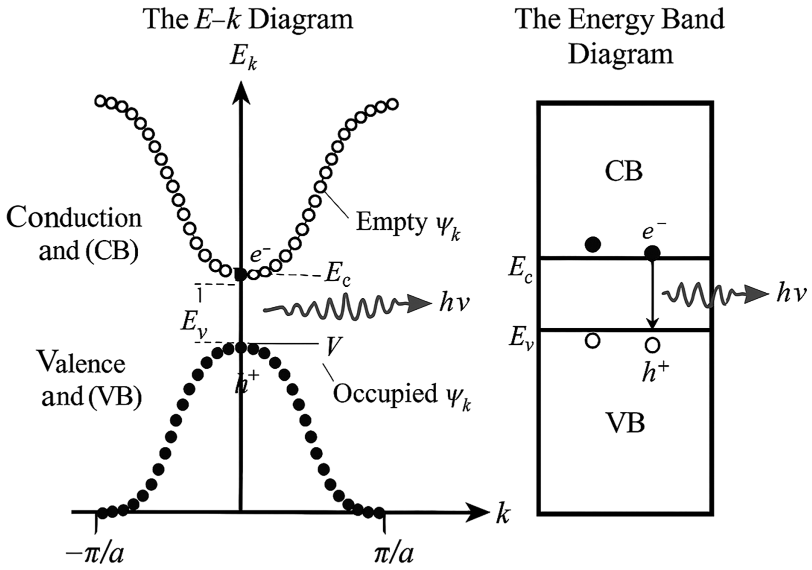

FIGURE 6.3 General pictorial representation of *E–k* diagram.

band. The effective mass of electrons in these valleys is higher, meaning they become harder to move, and thus, their mobility decreases. This phenomenon, called intervalley scattering, explains the nonlinear relationship between mobility and electric field at high values.

Thus, the entire current density now can be expressed as

$$\begin{aligned} J^{\text{total}} &= J_p^{\text{total}} + J_n^{\text{total}} = J_p^{\text{drift}} + J_p^{\text{diff}} + J_n^{\text{drift}} + J_n^{\text{diff}} \\ &= qN_p\mu_pE + qN_n\mu_nE - qD_p\frac{dN_p}{dx} + qD_n\frac{dN_n}{dx} \end{aligned} \tag{6.16}$$

6.2 EMPIRICAL MODELS

6.2.1 INTRODUCTION TO EMPIRICAL MODELS

Empirical models in semiconductor device physics are derived from experimental observations and data fitting rather than fundamental physical principles. They simplify the complex interactions within a device into manageable equations and parameters, which can be directly applied to practical device design and optimization. The reliance on empirical data makes these models particularly useful for established technologies where extensive experimental data are available.

The equations that describe current density—essentially how charges move—are often simplified versions of the Boltzmann Transport Equation (BTE). Based on the presumptions applied, distinct transport frameworks emerge, including the drift-diffusion (DD) model, the energy balance (EB) model, and the hydrodynamic approach. The model to be picked doesn't just affect charge movement—it also heavily influences the way of generation and recombination processes.

The DD model is one of the most widely used empirical models for simulating charge transport in semiconductor devices [25]. It combines two primary mechanisms of carrier transport: drift, resulted from electric fields, and diffusion, driven by carrier concentration gradients. The DD model is governed by *Continuity Equations for Electrons and Holes that* takes into account electron and hole densities, diffusion coefficients, mobilities, electric field, the generation rate, and the recombination rate, while Poisson's equation considers dielectric constant, electrostatic potential, charge and ionized donor and acceptor concentrations for electrostatic calculations [26].

The hydrodynamic and EB models extend the DD model by including additional transport phenomena such as carrier temperature and energy transport. These models account for non-equilibrium effects and provide more accurate descriptions of high-field and high-frequency behaviors [27]. While the hydrodynamic model incorporates the electron velocity and pressure tensor in its framework, the EB model focuses on variables such as energy density, heat flux, and rates of energy exchange.

Mobility models describe how the mobility of charge carriers varies with factors such as doping concentration, electric field, and temperature. The Caughey–Thomas model is a widely used empirical mobility model consisting minimum mobility, low-field mobility, doping concentration, reference doping concentration, and empirical fitting parameter [28]. This model accounts for mobility degradation due to increased impurity scattering at high doping levels.

6.2.2 DRIFT-DIFFUSION (DD) MODEL

We have detailed the current density equation in previous section (Equation 6.16) where the drift term ($J_p^{\text{drift}} + J_n^{\text{drift}}$) describes the carrier movement under influence of electric field. The diffusion ($J_p^{\text{diff}} + J_n^{\text{diff}}$) accounts for the carrier movement due to concentration gradients. In continuation of that, the fundamental equations governing the DD model are derived from the continuity equation, the Poisson equation for electrons and holes.

Continuity Equation ensures the conservation of the charge and is given separately for electrons and holes as

$$\frac{\partial N_p}{\partial t} = -\frac{1}{q}\nabla \cdot J_p^{\text{total}} + G_p - R_p \tag{6.17}$$

$$\frac{\partial N_n}{\partial t} = \frac{1}{q}\nabla \cdot J_n^{\text{total}} + G_n - R_n \tag{6.18}$$

where G_p and G_n: generation rates, R_p and R_n: recombination rates for holes and electrons respectively.

The Poisson equation relates the electric potential ψ to the charge distribution within the semiconductor as:

$$\nabla \cdot (\epsilon \nabla \psi) = -q(N_p - N_n + N_D{}^{+} - N_A{}^{-}) \tag{6.19}$$

where ϵ: permittivity, $N_A{}^-$ and $N_D{}^+$: ionized acceptor and donor concentrations respectively. Other terms bear identical meaning as in Section 6.1.

These equations collectively describe how charge carriers move within a semiconductor and how this movement generates an electric current. However, the DD model is based on several key assumptions that simplify the complex nature of charge transport. The principle of quasi-neutrality posits that charge carriers distribute themselves so that the net charge density remains almost balanced, except in regions like the depletion zone of a p–n junction where space charge effects become prominent. Low-Field Approximation presumes that the electric field is not much high, so the carrier mobility can be considered constant. This assumption breaks down in high-field regions, such as those near drain terminals in field effect transistors (FETs) and presumes that carriers stays in local equilibrium with the electric field and concentration gradients. This assumption allows the model to use local quantities like mobility and diffusion coefficients. Often, the DD model is applied under steady-state conditions where the time derivative terms in the continuity equations can be neglected. This is particularly useful in DC analysis of devices. The DD model originates from simplifying the BTE using the relaxation time approximation, which assumes that carrier distributions remain close to thermal equilibrium.

The DD model has been extensively used in the analysis and design of various types of FETs, including Metal-Oxide-Semiconductor FETs (MOSFETs) [29], FinFETs [30], and tunnel FETs (TFETs) [31]. It predicts the current-voltage characteristics, threshold voltage, subthreshold behavior, and short-channel effects. The model is valuable in analyzing how alterations in parameters like channel length, oxide thickness, and doping levels impact the overall performance of a device. The DD model is heavily utilized in optimizing FET designs for specific applications. For instance, it helps in tuning the doping profiles and gate work functions to achieve the desired trade-off between drive current and leakage current in low-power applications.

6.2.3 Hydrodynamic and Energy Balance Models

As semiconductor devices carry on to scale down in size at the same time increase in complexity, traditional models like the DD model, which assumes constant carrier mobility and neglects significant energy variations, can fall short, especially in high-field conditions where non-equilibrium effects become pronounced. To address these limitations, superior empirical models viz. the hydrodynamic and EB models have been developed. These models incorporate the effects of carrier energy and temperature, providing a more accurate description of charge transport under extreme conditions by including additional physical parameters that account for the variations in carrier energy and temperature.

a. **Energy Balance Model**:

A more advanced solution to the BTE connects the flow of current to the temperature or energy distribution of the carriers. The Energy Balance Transport Model, building on Stratton's derivation, takes the BTE to the next level [32]. It introduces continuity equations specifically for carrier temperatures, which means we're not just tracking charge anymore, but energy too! Instead of linking mobilities and impact ionization coefficients to the local electric field, this model ties them to the carrier temperatures [33].

From continuity equation, we have

$$J_p^{\text{total}} = qN_p\mu_p E - qD_p \frac{dN_p}{dx} \tag{6.20}$$

$$J_n^{\text{total}} = qN_n\mu_n E + qD_n \frac{dN_n}{dx} \tag{6.21}$$

To couple the current density with temperature and energy flux, the following modifications are done:

$$J_p^{\text{EB}} = qN_p\mu_p E - qD_p \frac{dN_p}{dx} - qN_p D_p^{\,T} \frac{dT_p}{dt} \tag{6.22}$$

$$J_n^{\text{EB}} = qN_n\mu_n E + qD_n \frac{dN_n}{dx} + qN_n D_n^{\,T} \frac{dT_n}{dt} \tag{6.23}$$

And,

$$S_p = -K_p \frac{dT_p}{dt} - \left[\frac{k\delta_p}{q}\right] J_p^{\text{EB}} T_p \tag{6.24}$$

$$S_n = -K_n \frac{dT_n}{dt} - \left[\frac{k\delta_n}{q}\right] J_n^{\text{EB}} T_n \tag{6.25}$$

where T_p and T_n are temperature for hole and electron, S_p and S_n are energy flux from carrier toward lattice, and K_p and K_p are hole and electron thermal conductivities, respectively.

$$D_p^{\,T} = \frac{\mu_p k T_p}{q} \frac{F_{1/2}\left\{F_{1/2}^{\;-1} \dfrac{N_p}{N_V}\right\}}{F_{-1/2}\left\{F_{1/2}^{\;-1} \dfrac{N_p}{N_V}\right\}} \tag{6.26}$$

$$K_p = qN_p\mu_p \left(\frac{k}{q}\right)^2 \Delta_p T_p \tag{6.27}$$

$$D_n^{\,T} = \frac{\mu_n k T_n}{q} \frac{F_{1/2}\left\{F_{1/2}^{\;-1} \dfrac{N_n}{N_C}\right\}}{F_{-1/2}\left\{F_{1/2}^{\;-1} \dfrac{N_n}{N_C}\right\}} \tag{6.28}$$

$$K_p = qN_n\mu_n\left(\frac{k}{q}\right)^2 \Delta_n T_n \tag{6.29}$$

k is the Boltzmann constant, $F_{1/2}$ is the Fermi function, and N_V and N_C are valance and conduction band state density. Remaining terms are similar as denoted in previous sections.

ζ_p and ζ_n are carrier temperature-dependent parameters, and based on the assumptions we make, the models differ. For example, taking ζ_p and $\zeta_n = -1$ at high field, velocity saturation limit, leads to Energy Balance Transport Model, whereas, taking ζ_p and $\zeta_n = 0$ would yield hydrodynamic model.

In an FET, these equations are only solved in the semiconductor region, while at the contacts, the electron and hole temperatures align with the lattice temperature of the contacts, keeping everything in thermal harmony. Meanwhile, on the other parts of the boundary that is other than contacts, the energy flux components vanish.

The models are particularly useful for simulating short-channel devices, where high electric fields cause significant deviations from equilibrium conditions, leading to effects such as velocity saturation, hot carrier injection, and impact ionization.

6.2.4 EMPIRICAL MOBILITY MODELS (E.G., CAUGHEY–THOMAS MODEL)

Electrons and holes resemble runners on a track—they're propelled by electric fields but continuously lose momentum due to interactions with lattice vibrations (phonons), impurity ions, other charge carriers, surface irregularities, and material flaws. These microscopic hurdles get rolled into macroscopic properties we call "mobilities," which depend on local conditions like electric field as well as lattice temperature, and doping concentration.

Mobility modeling breaks down into four main categories:

1. **Low-Field Behavior**: In regions where charge carriers are almost aligned with the lattice dynamics, their mobility settles into a typical low-field value, influenced mainly by phonon and impurity scattering. The empirical models used here are:
    - **The Caughey–Thomas Model**: is widely used for modeling *low-field mobility* as function of doping concentration in semiconductors [34].
    - **The Masetti Model** extends the Caughey–Thomas model, including doping dependence of carrier mobility at high doping concentrations and accounting for temperature dependence. It [35].
    - **The Arora Model** empirically relates carrier mobility to both doping concentration and temperature. It accounts for impurity scattering and temperature dependence, with expressions capturing both majority and minority carriers [36].
    - **Conwell–Weisskopf Model** accounts for carrier mobility influenced by ionized impurity scattering, especially at low temperatures [37].

- **Klaassen's Model** unifies multiple scattering mechanisms, including lattice, impurity, and carrier-carrier scattering [38].
- **Uchida's Low-Field Model for Ultrathin SOI** is specifically designed for ultrathin silicon-on-insulator (SOI) structures, where quantum confinement effects significantly alter mobility [39].

2. **High-Field Behavior**: Here, the mobility reduces with the field, as energetic carriers are exposed to more scattering processes. Eventually, mobility reaches a saturation velocity (νsat), mostly a function of the lattice temperature. Here are few commonly used models for high-field carrier mobility:
   - **Dorkel and Leturcq Model** primarily focuses on high-field mobility behavior, providing a semi-empirical relationship between carrier mobility and electric field [40].
   - **Caughey–Thomas Empirical Model** extends to high-field conditions by reducing mobility as the electric field increases, capturing the evolution from low-field to high-field saturation behavior [41].
   - **The Canali Model** describes high-field carrier mobility by incorporating velocity saturation effects [42].
   - **The Herring–Vogt Model** is utilized to describe anisotropic high-field mobility, accounting for the variation in carrier velocity along different crystallographic directions in semiconductors, such as in materials like silicon and gallium arsenide [43].
3. **Bulk Regions**—which involve modeling how hole, electron mobility and saturation velocity of them vary with doping and temperature and how to describe the transition between low-field and saturation behaviors. One common analytical expression for mobility in bulk semiconductors is the Arora model:

$$\mu\left(T, N_{\text{Doping}}\right) = \mu_0\left(\frac{T}{T_0}\right)^{-\gamma}\left(\frac{N_{\text{Doping}}}{N_0}\right)^{-\delta} \tag{6.30}$$

   where μ_0 is the mobility at reference temperature T_0, T is the temperature of lattice, N_{Doping} is the doping concentration, and γ and δ are fitting parameters.
4. **Inversion Layers**—where things get more complicated due to surface scattering, carrier-carrier interactions, and quantum size effects. These phenomena are often gauged by the transverse electric field. The *Sakaki model* is often used to describe mobility in inversion layers, where mobility is dependent on the transverse electric field:

$$\mu\left(E\perp\right) = \frac{\mu_0}{1+\beta E\perp^{\gamma}} \tag{6.31}$$

   μ_0 is the low-field mobility, $E\perp$ is the transverse electric field, and β and γ are empirical fitting parameters to account for surface scattering effects.

6.2.5 PARAMETER EXTRACTION AND FITTING

Parameter extraction and fitting involve the process of calibrating empirical models to align with experimental data. In the realm of electronic components like transistors, particularly field effect devices (FETs), this step is crucial for ensuring that model parameters accurately represent real-world charge transport phenomena. By adjusting these parameters, the model can be fine-tuned to reflect specific device characteristics, such as mobility, carrier concentration, or doping levels. Effective parameter extraction requires careful optimization to minimize errors between the model predictions and experimental results, providing a more reliable framework for device simulation and analysis.

6.2.6 ADVANTAGES OF EMPIRICAL MODELS: SIMPLICITY AND COMPUTATIONAL EFFICIENCY

Empirical models offer notable advantages, particularly in terms of simplicity and computational efficiency. These models are often based on experimental data, allowing them to bypass complex physical equations and instead use fitted parameters to predict device behavior. This simplicity makes empirical models easier to implement and less resource-intensive compared to more detailed theoretical models. As a result, they can quickly provide useful insights into device performance, making them especially valuable in large-scale simulations and early-stage design processes where computational speed is crucial.

6.2.7 LIMITATIONS: RELIANCE ON EXPERIMENTAL DATA, LESS PREDICTIVE POWER

Empirical models offer clear advantages such as simplicity and computational efficiency, making them well-suited for practical device simulations. However, their limitations include a heavy reliance on experimental data, which means their predictive power is often limited to conditions where data is available. Consequently, these models may struggle to accurately predict behavior in new or extreme scenarios where experimental validation is lacking.

6.3 QUANTUM CORRECTIONS TO CLASSICAL MODELS

6.3.1 INTRODUCTION TO QUANTUM CORRECTIONS TO CLASSICAL MODELS

The *DD model* has been the cornerstone of transport modeling in semiconductors for many decades. This framework relies on a collection of partial differential equations that outline how charge carriers (electrons and holes) move due to applied electric fields (drift) and spread out because of differences in their concentration (diffusion). The DD model works well for devices with relatively large geometries (micron scale) where quantum mechanical effects are negligible, and it remains the standard model for macroscopic device simulations [44].

The rapid miniaturization of semiconductor devices, as foreseen by the Semiconductor Industry Association (SIA), has brought forth a multitude of challenges in device modeling and simulation [45]. Modern semiconductor devices such as High Electron Mobility Transistors (HEMTs), Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs), and Resonant Tunneling Diodes (RTDs) operate on the decanano length scale (below 50 nm), where quantum mechanical effects become significant [46]. This miniaturization has necessitated the inclusion of quantum mechanical phenomena, such as confinement, tunneling, and quantum charge transport, which classical models are unable to account for adequately. Quantum corrections to classical models provide a pathway to bridge the gap between classical descriptions and quantum mechanical behavior, ensuring that simulations remain computationally efficient while incorporating essential quantum effects.

However, as devices have shrunk to nanometer scales, this model faces limitations. In particular, the DD model assumes a continuum of charge carriers, neglecting quantum effects such as wave-like behavior and quantum confinement in the inversion layers of MOSFETs or tunneling through potential barriers. To address these deficiencies, *quantum corrections* are necessary, allowing the inclusion of quantum effects into otherwise classical models [47].

- When the dimensions of the device become comparable to the *de Broglie wavelength* of charge carriers, the carriers are confined in potential wells, such as the inversion layer in MOSFETs. This results in the quantization of energy levels, which cannot be captured by classical models [48].
- At very small gate oxide thicknesses (on the order of a few nanometers), electrons can *tunnel* through the oxide barrier in MOSFETs, leading to gate leakage [49]. This quantum tunneling is ignored by classical models but has significant implications for power consumption and device reliability.
- The transport of charge carriers is no longer dominated purely by drift and diffusion mechanisms but involves *quantum mechanical interference and phase coherence effects* [50]. Classical models fail to describe such behavior.

Quantum-corrected models such as the Schrödinger–Poisson Self-Consistent (SP) model, Quantum Hydrodynamic (QHD), and Quantum Energy Transport (QET) models are essential in accurately simulating carrier behavior in confined regions. The Quantum Drift-Diffusion (QDD) and Van Dort–Hansch models extend classical transport models by incorporating quantum corrections, while the DG and Bohm Quantum Potential (BQP) models provide robust frameworks for quantum confinement and tunneling effects.

In the following section, we will discuss these models in detail, highlighting their applications, advantages, and limitations in modeling quantum effects in nanoscale devices.

6.3.2 QUANTUM HYDRODYNAMIC (QHD) MODELS

To reduce computational complexity, macroscopic models incorporating quantum effects have been developed. The *quantum hydrodynamic* (*QHD*) *model* is one such example [51–54]. The *QHD* model emerged as a natural quantum extension of classical hydrodynamic models. It was developed to describe quantum transport phenomena using fluid-like equations for quantities such as density, *current*, and *energy* [55]. The foundation of the QHD model is the *Madelung transformation*, which rewrites the Schrödinger equation in a form similar to hydrodynamic equations. Over time, QHD has become popular in modeling *quantum systems* such as *semiconductors* and *plasmas* [56].

The relationship between QHD models and the BQP is fundamental, as the Bohm potential is crucial in incorporating quantum effects into the hydrodynamic framework. This potential helps account for phenomena such as quantum tunneling and non-local behaviors, enabling QHD models to extend classical hydrodynamics into the quantum regime. By including quantum corrections like DG effects, the Bohm potential allows QHD models to provide more accurate descriptions of quantum systems, including transport and electromagnetic field interactions in nanostructures and plasmas. These models find applications in semiconductor physics and quantum fluids, and their evolution will continue as quantum effects become increasingly relevant in nanoscale systems [57–59].

The *BQP* method is a quantum mechanical model used in device simulations to account for these effects. It is based on the *Bohm interpretation of quantum mechanics* and has been implemented in tools such as *Silvaco's Atlas*. This approach provides an alternative to the *DG method* and is especially useful for simulations involving quantum confinement and tunneling effects.

The BQP introduces a position-dependent quantum potential, *Q*, which modifies the potential energy of carriers (electrons or holes) in the device. This modification allows the model to account for quantum effects in a way that is computationally efficient and can be calibrated against more rigorous quantum mechanical models, such as the *Schrödinger–Poisson equation*.

The concept of the quantum potential originated with David Bohm, who introduced it as part of his alternative interpretation of quantum mechanics. This approach was designed to incorporate the quantum effects that are typically neglected in classical physics. Over time, the BQP concept has been refined to account for various quantum phenomena, such as quantum tunneling, quantum confinement, and non-equilibrium quantum transport. These refinements have enriched the model's theoretical framework and its application to semiconductor device simulations.

While the BQP model was historically linked to Madelung's hydrodynamic formulation, it has since evolved to be distinct from both the QHD and QDD models. The BQP model integrates quantum effects directly into the potential term, allowing for more accurate simulations without needing the assumptions and corrections typical in QHD and QDD models.

QHD models describe electrons as a *quantum fluid*, incorporating essential quantum effects such as *quantum tunneling* and *quantum pressure* through quantum corrections to classical fluid equations [60]. The model finds significant application in studying semiconductor devices where the *size of the system is comparable to the electron wavelength*, leading to quantum confinement effects.

The QHD model is derived by transforming the *Schrödinger equation* into hydrodynamic-like equations that describe the flow of electron density and current. This transformation is done using the *Madelung transformation*, which rewrites the Schrödinger equation in terms of a fluid's density and velocity.

6.3.2.1 Assumptions

- Electrons are treated as a *fluid* governed by quantum-corrected Navier–Stokes-like equations.
- The wave function is expressed in polar form, where the phase of the wave function is related to the particle's velocity. This transformation is valid as long as the wave function remains single-valued and well-behaved.
- The model includes quantum effects through a *quantum pressure term* derived from the Bohm potential.
- Self-consistency with *Poisson's equation* ensures that electrostatic forces are properly accounted for.

6.3.2.2 Key Concept

The *Madelung transformation* is the fundamental mathematical basis for deriving QHD from quantum mechanics. This transformation rewrites the *Schrödinger equation* in a form analogous to classical hydrodynamics by expressing the wave function $\psi(r,t)$ in polar form [61–63]:

$$\psi(r,t) = \sqrt{n(r,t)e^{iS(r,t)/\hbar}} \tag{6.32}$$

Here $n(r,t)$ is the electron density, $S(r,t)$ is the action related to the velocity, and $\hbar$ is the reduced Planck constant.

Substituting this expression into the *time-dependent Schrödinger equation* [64]:

$$i\hbar\frac{\partial\psi}{\partial t} = \left[-\frac{\hbar^2}{2m*}\nabla^2 + V(r,t)\right]\psi \tag{6.33}$$

and separating the real and imaginary parts, we get two coupled equations: the *continuity equation* and the *quantum Euler equation.*

6.3.2.2.1 Real Part

The real part of the Schrödinger equation provides the *quantum Euler equation*, which resembles the *momentum conservation equation* from classical fluid mechanics but includes a correction due to *quantum pressure*:

$$m\left(\frac{\partial v}{\partial t} + v\cdot\nabla v\right) = -\nabla V - \frac{\nabla P}{n} + F_q \tag{6.34}$$

Here $V(r,t)$ is the external potential, P is the classical pressure term, and F_q is the *quantum force* resulting from the *quantum potential.*

The *quantum potential* V_q introduces a correction to the classical Euler equation and is given by

$$V_q = --\frac{\hbar^2\nabla^2\sqrt{n}}{2m*\sqrt{n}} \tag{6.35}$$

This quantum potential accounts for *quantum mechanical effects,* namely tunneling and *quantum pressure*, which arise due to the wave nature of particles. The term involving the Laplacian of the density provides a non-local interaction that makes the QHD model different from classical hydrodynamic models.

6.3.2.2.2 Imaginary Part

The result is the *continuity equation*, which governs the conservation of mass (or particle density) and is derived from the imaginary part of the Schrödinger equation [65]:

$$\frac{\partial n}{\partial t} + \nabla \cdot (nv) = 0 \tag{6.36}$$

where $n(r,t)$ is the electron density and $v(r,t) = \frac{1}{m}\nabla S$ is the velocity field resultant from the phase of the wave function.

This equation is structurally identical to the classical continuity equation used in fluid dynamics and describes the conservation of particles in the system.

6.3.2.3 Limitations

- Similar to other quantum models, QHD faces difficulties in simulating *large systems*, particularly due to computational costs.
- For devices where quantum *coherence and entanglement* play significant roles, QHD may not capture these effects with sufficient accuracy.
- Implementing correct *boundary conditions* can be challenging, especially in devices with complex geometries.

6.3.3 QUANTUM ENERGY TRANSPORT (QET)

The *QET* model evolved from the *EB* framework commonly used in classical semiconductor device simulations [66,67]. QET modifies this by introducing quantum effects, such as *quantum confinement* and *quantum energy levels.* The quantum corrections to energy transport account for phenomena like *subband quantization* in confined systems, making the model suitable for nanoscale devices [68].

Classical models, such as Fourier's law, describe energy transport based on macroscopic quantities like temperature gradients and heat flux. However, at the nanoscale, where the dimensions of materials approach the electron's wavelength, quantum effects become significant.

QET builds upon the basics of *quantum mechanics* and *statistical mechanics*, particularly the principles governing the behavior of electrons in a material.

QET is founded on several key principles that differentiate it from classical energy transport theories as QET is the wave-particle duality of electrons and the quantum mechanical nature of their interactions [69,70]. The transport of energy is described using quantum states and wave functions, reflecting the probabilistic behavior of particles. The *Fermi–Dirac distribution* describes the tenancy of energy states by electrons at a given *temperature*, impacting the energy transport process. QET addresses the dynamics of energy transport in *non-equilibrium conditions*, where thermal gradients exist. This is essential for understanding heat flow in nanoscale devices, where temperature differences can drive energy transport. The preservation of *quantum coherence* in systems is critical for energy transport [71]. Quantum coherence affects how energy states are populated and influence the transport properties of materials.

This section explores the evolution of the QET model, its fundamental principles, analytical expressions, and derivations. It also addresses the assumptions and limitations of the model while discussing its applications in modern technology.

6.3.3.1 Assumptions

- The model assumes that carriers (electrons and holes) follow quantum-corrected EB equations, where quantum effects modify the carrier energy and heat generation.
- Like classical energy transport models, QET uses a semiclassical framework, with quantum corrections accounting for effects like *quantized energy states.*
- Self-consistent coupling with *Poisson's equation* provides electrostatic field and charge interactions.

6.3.3.2 Key Concept

The foundation of QET lies in the derivation of analytical expressions that describe the transport of energy in quantum systems. Here, we explore the key equations that govern energy transport at the quantum level.

6.3.3.2.1 The Quantum Boltzmann Transport Equation

The Quantum Boltzmann Transport Equation (QBTE) is a fundamental equation in QET that describes the distribution function of particles in phase space [72]. It incorporates quantum mechanical effects into the classical BTE, providing insights into how energy is distributed and transported.

The QBTE can be expressed as follows:

$$\frac{\partial f(r,k,t)}{\partial t}+\frac{F}{\hbar}\cdot\nabla_r f+\frac{k}{\hbar}\dot{}\cdot\nabla_k f=\left(\frac{\partial f}{\partial t}\right)_{\text{coll}} \tag{6.37}$$

where

- $f(r,k,t)$ is the distribution function in phase space,
- F is the external force acting on the particles,
- K is the rate of change of the wave vector k,
- $\left(\frac{\partial f}{\partial t}\right)_{\text{coll}}$ represents the collision term accounting for scattering processes.

6.3.3.2.2 Energy Transport Equation

In the context of QET, the energy transport can be described using a continuity equation similar to the classical form but incorporating quantum corrections [73,74]. The energy transport equation can be expressed as

$$\frac{\partial E}{\partial t} + \nabla \cdot J_E = 0 \tag{6.38}$$

The total energy density E in the system can be expressed in terms of the particle density n and the kinetic energy

$$E = n\left(\frac{1}{2}mv^2 + U\right) \tag{6.39}$$

where U stands for the potential energy in the system.

J_E is the energy flux density can be derived as

$$J_E = \frac{1}{2}n(r,t)v^2 + \frac{\pi 2}{4}k_B T^4 \tag{6.40}$$

where E is the energy density, J_E is the energy flux density, $n(r,t)$ is the particle density, v is the velocity of the particles, k_B is the Boltzmann constant, and T is the temperature.

The QET coefficient kappa can be expressed in terms of the particle density, temperature, and scattering rates:

6.3.3.3 Limitations

- While QET introduces quantum corrections, it does so in a semiclassical manner, which *may not be accurate* for devices operating in strong quantum regimes.
- QET may *fail in regions with strong electric fields* or rapidly varying potentials where quantum coherence dominates transport behavior.
- The model may not account for *non-ideal behaviors* such as disorder, localized states, or strong electron correlations that can significantly impact energy transport.

Quantum Transport Equations (QTEs) and QHD are interconnected frameworks aimed at describing quantum systems, each addressing different aspects of quantum dynamics while sharing foundational principles. QTEs model the dynamics of particles, such as electrons, focusing on the redistribution of energy and momentum among them, which is essential for understanding transport properties in semiconductor physics and device operation. In contrast, QHD treats quantum systems as fluids, utilizing concepts from classical fluid dynamics to describe the collective behavior of quantum particles, capturing phenomena like superfluidity and quantum turbulence. The relationship between QTE and QHD is evident through their overlapping fields, as QHD can be derived from the BTE that underlies QTEs, creating a direct connection. Essentially, while QTEs emphasize particle transport dynamics, QHD offers a macroscopic perspective in fluid dynamics. This synergy allows for a comprehensive analysis of electron transport in semiconductor devices, where both quantum mechanics and hydrodynamic principles are vital. In practical applications, researchers leverage both frameworks to enhance the performance of nanoscale devices, with QHD modeling macroscopic material properties influenced by quantum effects, and

QTE providing detailed insights into electron behavior, ultimately leading to better designs for electronic and optoelectronic devices.

6.3.4 QUANTUM DRIFT DIFFUSION (QDD)

The *QDD model (QDDM)* incorporates quantum corrections into the classical DD model, which introduces a quantum correction term to account for quantum confinement and tunneling effects. The QDDM maintains the computational efficiency of the classical DD model while including quantum effects.

The QDDM is particularly useful in MOSFETs, where quantum confinement in the inversion layer significantly alters carrier distribution. The inclusion of the quantum correction term allows for a more accurate description of carrier densities near the Si/SiO$_2$ interface.

6.3.4.1 Assumptions

- *Quantum confinement effects* are included in the DD equations by introducing correction factors for carrier concentration and mobility.
- The *potential energy landscape* is smooth, but quantum mechanical tunneling and quantization effects are incorporated through effective correction terms.
- Self-consistency is maintained by coupling with the *Poisson equation* for electrostatic potential.

6.3.4.2 Key Concept

The QDDM was developed by Degond et al. to effectively describe the diffusive behavior of quantum particles [75]. This model addresses the limits of the classical DD model, which becomes increasingly inaccurate as electronic device sizes shrink. Thus, it is crucial to incorporate models that account for quantum effects.

The QDDM is derived as the diffusive limit of the quantum Liouville–Bhatnagar-Gross-Krook equation (BGK) equation.

We start from quantum master equation, which governs the time evolution of the density matrix ρ of a quantum system [76]. This type of equation is used to describe open quantum systems, where the system interacts with its environment, leading to both coherent (unitary) evolution and non-coherent (dissipative) processes.

$$i\frac{\partial \rho}{\partial t} = [H, \rho] + iQ(\rho) \tag{6.41}$$

$\frac{\partial \rho}{\partial t}$ is the *time derivative* of the density matrix ρ. It represents the *rate of change* of the system's density matrix, which contains all the statistical information about the quantum state of the system, including probabilities and coherences (superpositions). It is noted that the density matrix ρ is used to describe both pure and mixed quantum states [77]. It encapsulates the *coherent* (*unitary*) *evolution* of the quantum system, following the Schrödinger equation for pure states or the von Neumann equation for mixed states. $[H,\rho]$ is the *commutator* between the Hamiltonian H and the density matrix ρ [78]. The term $iQ(\rho)$ represents the *dissipative* or *non-unitary* part of the evolution, which is due to the interaction of the system with its environment [79]. $Q(\rho)$ is an operator that describes the *environmental effects* (e.g., decoherence, dissipation, relaxation) acting on the density matrix ρ. It captures how the system loses information to its surroundings, such as when a quantum system interacts with a thermal bath or other external noise sources. Q is of the BGK type and is expressed in its simplest form as [80]:

$$Q(\rho) = \frac{1}{\tau}(e(\rho) - \rho) \tag{6.42}$$

where τ is the relaxation time, and $e(\rho)$ represents the quantum statistical equilibrium. The primary motivation behind these equations is to depict the collective dynamics of many-particle quantum systems and to derive reduced quantum fluid models. To achieve this, Degond and Ringhofer adapted Levermore's entropy closure strategy to the quantum context [81].

The *particle density* $n(r,t)$ is the diagonal element of the density matrix ρ in the position basis:

$$n(r,t) = \left\langle r \middle| \rho(t) \middle| r \right\rangle \tag{6.43}$$

In other words, the *local particle density* at position r and time t is given by the expectation value of the density matrix at that point.

Coherent Term (Unitary Evolution): The commutator $[H,\rho]$ describes the *coherent unitary evolution*. Using a Hamiltonian of the form

$$H = -\frac{\hbar^2}{2m*}\nabla^2 + V(r) \tag{6.44}$$

where $V(r)$ the potential energy, the commutator can be expanded to give a *quantum Liouville equation*. For the particle density n, this results in a contribution that governs the *drift* of particles under the influence of the potential $V(r)$.

This drift is associated with the quantum mechanical wavefunction evolution.

Combining the coherent evolution from the quantum Hamiltonian with the dissipative dynamics from $Q(\rho)$ and making the appropriate approximations, we arrive at the *QDD equation* [82]:

$$\frac{\partial n}{\partial t} - \nabla \cdot \left(n\nabla \frac{\delta F[n]}{\delta n} \right) = 0 \tag{6.45}$$

This equation describes the *time evolution* of the particle density $n(r,t)$ under the influence of quantum effects (via the free energy functional $F[n]$) as well as classical drift and diffusion. The functional derivative $\delta F[n] / \delta n$ represents the effective potential or force driving the flow of particles.

6.3.4.3 Limitations

QDD is inherently a semiclassical approximation, and as such, it is less accurate in highly quantum systems where full quantum mechanical treatments (like Non-Equilibrium Green's Function (NEGF)) are needed. For very small devices or strong confinement regimes, QDD may not capture all important quantum effects, particularly *coherent transport* [83]. Moreover, QDD struggles to accurately model *quantum tunneling*, as it relies on approximations for both carrier concentration and potential energy.

6.3.5 Van Dort, Hansch, and Improved Local Density Approximation (IMLDA) Models

The Van Dort and Hansch models play a pivotal role in enhancing semiconductor device simulations by incorporating quantum mechanical effects into classical models like the QDDM. Their relevance stems from the need to address quantum confinement, tunneling, and the behavior of charge carriers in highly scaled devices such as MOSFETs, where classical simulations fall short.

6.3.5.1 Van Dort Model

The Van Dort model accounts for quantum mechanical effects by widening the energy bandgap (ΔE) in the inversion channel of MOSFETs, specifically addressing the reduction in the density of states caused by quantum confinement [84]. This model adjusts the conduction band edge as a function of the perpendicular electric field near the gate oxide interface. The formula

$$\Delta E_g = \frac{13}{9}\beta(\kappa_{Si} 4qkBT)^{1/3} \left| E \perp \right|^{2/3} \tag{6.46}$$

corrects for quantum mechanical carrier behavior, but it occasionally results in unphysical outcomes, such as an excess of electron concentration near the oxide interface. Despite this limitation, the Van Dort model is valuable for modeling capacitance–voltage (C–V) characteristics in nanoscale devices.

6.3.5.2 Hansch Model

The *Hansch model*, originally developed for quantitative structure–activity relationship (QSAR) analysis in medicinal chemistry, is a mathematical approach that helps relate chemical structure to biological activity [85]. In the context of semiconductor device physics, its adaptation provides a way to incorporate *quantum mechanical corrections* into simulations of charge transport and device behavior at the nanoscale [86]. This extension of the Hansch model helps better account for the *quantum confinement effects* in modern semiconductor devices, like MOSFETs, where the classical models struggle.

In semiconductor devices at the nanoscale, quantum effects become prominent due to the confinement of electrons and the formation of quantum wells. Classical models tend to overestimate carrier densities near the interface of semiconductors and insulators (like Si/SiO$_2$ in MOSFETs). The Hansch model corrects this by introducing quantum mechanical considerations. The confinement causes quantization of energy levels, leading to a modified *density of states* and an effective increase in the *bandgap energy*. The Hansch model accounts for these shifts to make the simulated behavior closer to reality.

In the adaptation of the Hansch model to semiconductors, certain *quantum descriptors* are utilized. These quantum descriptors are metrics that characterize the quantum mechanical nature of the system, such as [87]:

- *Electron wavefunctions* in confined structures (quantum wells)
- *Energy eigenstates* of the carriers (electrons/holes) within the semiconductor
- *Carrier concentration near interfaces*, where the quantum confinement is strongest

While the exact mathematical form of the Hansch model in semiconductor physics may differ depending on the specific application, the general approach involves modifying the classical DD equations by adding *corrections based on quantum mechanical principles*.

For example, in the context of a MOSFET, the quantum correction factor introduced by the Hansch model would modify the *electron density profile* near the gate oxide interface [88–90]:

$$n_q(z) = n_c(z) \times \exp\left(-\frac{E_g{}^q(z)}{k_B T}\right) \tag{6.47}$$

$n_q(z)$ is the quantum-corrected electron density at position z; $n_c(z)$ is the classically predicted electron density; $E_g{}^q$ is the quantum-corrected bandgap energy, which depends on factors like gate electric field and oxide thickness; k_B is Boltzmann's constant; and T is the temperature.

6.3.5.3 Improved Local Density Approximation (IMLDA) in Semiconductor Devices

In semiconductor physics, quantum effects become increasingly important as devices shrink to the nanometer scale. The *Local Density Approximation* (*LDA*) and its improved version, the *Improved Local Density Approximation* (*IMLDA*), are essential tools for addressing these quantum mechanical effects in semiconductors, particularly in MOSFETs and other devices that operate at extremely small scales [91].

The *IMLDA* enhances the standard LDA by providing better approximations for quantum mechanical corrections in device simulations [92]. It modifies the potential and charge distribution in quantum-confined regions, helping to capture the physical reality of how electrons and holes behave at these small dimensions. In this extended analysis, we'll explore the theory behind the IMLDA, its mathematical framework, and its relevance to modern semiconductor devices.

Before diving into the IMLDA, it's important to understand the *LDA*. In the LDA approach, quantum mechanical corrections to carrier densities and potentials are applied based on the *local electron density* in the device [93]. This method uses *quantum statistical mechanics* principles to adjust the behavior of charge carriers near interfaces, typically between a semiconductor and an insulator, like in a MOSFET.

The LDA assumes that the system can be treated as locally homogeneous. Although the device as a whole (like a transistor) is nonuniform due to differences in dopant levels or electric field distributions, each specific location can be treated as if it exhibits uniform properties. The LDA introduces a *quantum correction potential* to the classical Poisson equation, aiming to account for quantum mechanical effects such as the *quantum confinement* of carriers in potential wells [94].

The Poisson equation for a semiconductor can be written as

$$\nabla \cdot \epsilon \nabla \psi = -q(p - n + N_D{}^{+} - N_A{}^{-}) \tag{6.48}$$

where ϵ: permittivity of the material. ψ: electrostatic potential. q: charge. n and p are the electron and hole concentrations, respectively. $N_D{}^{+}, N_A{}^{-}$ are the concentrations of ionized donors and acceptors, respectively.

The LDA corrects this equation by adding a *quantum correction potential*, $V_q(r)$ to account for the quantum confinement of electrons:

$$\nabla \cdot \epsilon \nabla \psi = -q(p - n + N_D{}^{+} - N_A{}^{-}) + V_q(r) \tag{6.49}$$

The LDA has limitations when applied to *modern nanoscale devices*, such as *FinFETs*, *SOI MOSFETs*, and *quantum wells* [95]. One of the main shortcomings of the LDA is its inability to accurately predict the behavior of electrons near surfaces or interfaces, where strong quantum effects come into play. For example, in the case of *MOSFETs with ultrathin gate oxides*, LDA tends to overestimate the electron density near the *Si/SiO$_2$ interface*, leading to unphysical results such as *electron pileup* at the boundary.

The *IMLDA* was developed to address these issues by improving the approximation of quantum mechanical effects in inhomogeneous systems [96,97]. Specifically, it corrects for the limitations of LDA in regions of steep potential changes (such as near interfaces) by using a more sophisticated treatment of the quantum correction potential. In IMLDA, the quantum correction potential is computed by solving the *DG equation*, which is a higher-order approximation that accounts for the *spatial variation* of the electron density.

In IMLDA, the carrier density is computed by solving the *Schrödinger equation* for confined electrons and using the resulting wavefunctions to calculate the local carrier density [98]. For example, in a MOSFET with an ultrathin gate oxide, the electron density near the interface is given by

$$n(r) = \sum_{i} \left|\psi i(r)\right|^2 f(Ei) \tag{6.50}$$

where $\psi i(r)$ is the wavefunction of the *i*th energy level, obtained by solving the Schrödinger equation. $f(Ei)$ is the Fermi–Dirac distribution, which describes occupancy of the energy level Ei.

The *wavefunctions* and *energy levels* are determined by solving the Schrödinger equation with the *self-consistent potential* obtained from the Poisson equation. This ensures that the carrier densities are correctly computed, taking into account both the *electrostatic potential* and the *quantum confinement effects*.

6.3.5.4 Comparison of Quantum Correction Models

In comparison to other models like the *Van Dort model* or the *IMLDA*, the Hansch model can be seen as complementary:

- **Van Dort Model**: Primarily focuses on the correction of the *energy band structure* due to perpendicular electric fields and quantum confinement, but may introduce unphysical increases in electron density near interfaces.
- **Hansch Model**: Incorporates quantum effects more holistically, using quantum mechanical descriptors to provide a more nuanced correction to *both the band structure and the carrier density*. It aims to avoid the unphysical results seen in simpler models like Van Dort's.
- **IMLDA**: Improves on the limitations of classical *LDA* models, especially regarding the *electron distribution* near oxide interfaces, but may still lack the refinement offered by Hansch's quantum descriptors.

6.3.6 DENSITY GRADIENT (DG) MODEL

The *DG model* is a quantum correction model that modifies the classical *DD* equations by introducing a gradient of the electron density to account for *quantum mechanical effects* [99–102].

The DG model serves as a quantum enhancement of the classical DD framework. It adapts the classical equations by introducing an additional term based on the spatial gradient of carrier density, effectively incorporating quantum mechanical effects like wavefunction spreading. The DG model is often seen as an *approximation* to the full QHD model. It introduces quantum effects via the *gradient of the particle density* (which resembles the BQP), but it does not include full momentum transport equations like in QHD [103,104].

The *model* is a mathematical framework used to describe the transport phenomena of charged particles, particularly in semiconductor physics. It is often considered an extension or a correction of the classical DD model by incorporating quantum effects.

Developed in the context of *MOSFETs* and *high-mobility transistors* (*HEMTs*), the DG model has found widespread application in *nanoscale semiconductor device* simulations.

While *QHD model* is a more detailed and comprehensive model that includes quantum effects through hydrodynamic equations and the Bohm potential, *DG model* is a simplified, less computationally intensive model that adds quantum corrections to the classical DD equations without explicitly modeling momentum transport.

In the DD model, the transport equations for charge carriers are modified to explain quantum effects linked with the confinement of carriers and local potential disparity. These effects are crucial when the dimensions of the device are comparable to the wavelength of the carriers, leading to behaviors that classical models cannot capture effectively.

The DG model is derived from the moments of the *Wigner function*, which provides a quantum mechanical description of the statistical state of particles. This model modifies the carrier transport equations by including quantum correction terms that impact carrier current and energy flux [105–108].

6.3.6.1 Assumptions

- The quantum mechanical corrections are included through an additional term in the *DD equation* that takes into account the spatial variation of the carrier density (hence the name density gradient).
- This model assumes that quantum confinement and tunneling are important but can be captured by correcting the classical DD framework.
- *Poisson's equation* is used to calculate the electrostatic potential, ensuring that charge density and potential are self-consistent.

6.3.6.2 Key Concept

Quantum Correction Potential:

In the DG model, the expression for the electron current, originally described by classical equations, is replaced by a modified expression that includes a quantum correction potential, denoted as Λ. This correction accounts for the influence of quantum confinement on carrier dynamics [99].

$$J_n = qD_n\nabla_n + q_n\mu_n(-\nabla(\psi - \Lambda) + kT_L\nabla ln(n)) \tag{6.51}$$

Here J_n is the electron current density, q is the charge of the electron, D_n is the diffusion coefficient, n is the carrier concentration, μ_n is the mobility of electrons, ψ is the electrostatic potential, k is Boltzmann's constant, T_L is the lattice temperature.

The quantum potential Λ can be calculated using expressions

$$\Lambda = -\frac{\gamma\hbar^2\nabla^2\sqrt{n}}{6m*\sqrt{n}} \tag{6.52}$$

the above equations parameters incorporate a *fit factor* γ, the carrier effective mass m, and the appropriate carrier concentration n.

In *MOS capacitors* with thin gate oxides, the DG model helps in understanding the behavior of carriers under varying electric fields, particularly as dimensions shrink below a few nanometers. It allows for the analysis of *quantum capacitance* effects, which become significant in advanced technologies.

6.3.6.3 Limitations

While the DG model effectively incorporates quantum effects, it has limitations. The model is primarily valid under certain conditions, such as low carrier concentrations and specific geometries. Moreover, its reliance on fit factors requires careful calibration to match experimental data, which can introduce uncertainties.

Future advancements may involve integrating the DG model with more comprehensive quantum mechanical frameworks, such as *QHD*, to provide a more unified approach to quantum transport in semiconductor devices. Additionally, as device dimensions continue to shrink, further refinements in the model will be essential to account for emerging quantum phenomena, ensuring accurate simulations that drive the development of next-generation electronic and optoelectronic devices.

6.3.7 Monte Carlo, Effective Mass Approximation, (*k·p*), and Methods

Kinetic Monte Carlo (KMC) and Ensemble Monte Carlo (EMC) are computational techniques used to simulate carrier transport in materials and devices. KMC operates on a discrete-event framework, where individual carrier transitions are governed by transition rates, making it ideal for studying time-dependent phenomena such as defect trapping or reaction kinetics. EMC, in contrast, employs statistical sampling of carrier ensembles to solve the BTE, providing insights into high-field transport, scattering mechanisms, and non-equilibrium phenomena. Both methods bridge classical transport theory with quantum corrections, enabling accurate modeling of nanoscale devices while maintaining computational efficiency.

Both KMC and EMC are semiclassical models widely used for transport simulations. KMC focuses on individual stochastic events, simulating carrier dynamics through transition rates derived from semiclassical approximations, making it suitable for modeling trap-limited conduction or diffusion. EMC, on the other hand, statistically solves the BTE by simulating ensembles of carriers, effectively capturing high-field transport and scattering effects. While both methods primarily rely on classical trajectories, quantum corrections, such as effective mass or tunneling probabilities, can be incorporated. However, neither KMC nor EMC inherently models full quantum coherence or interference, distinguishing them from purely quantum approaches like NEGF.

The *k·p* method and the effective mass approximation (EMA), while not direct transport models, play vital roles in enabling semiclassical transport models to incorporate quantum mechanical effects in nanoscale semiconductor devices. The EMA simplifies the representation of electron and hole dynamics by assuming a constant effective mass averaged over the band structure, which is computationally efficient and sufficient for bulk materials or larger structures. However, as device dimensions shrink, quantum confinement effects, potential variations, and non-parabolicity in the band structure become significant, limiting the EMA's applicability.

To address these limitations, the *k·p* method provides a more detailed approach by incorporating band mixing and non-parabolicity. This method expands the electronic wavefunctions around critical points in the band structure, making it particularly effective for modeling electronic behavior near band edges in heterostructures and low-dimensional systems. These attributes are crucial for accurate predictions of energy levels, wavefunctions, and band structures in structures such as quantum wells, superlattices, and nanoscale FETs.

In the context of semiclassical transport, these methods complement each other. The EMA offers a straightforward framework for device-level simulations, while the *k·p* method refines effective mass parameters to incorporate quantum mechanical corrections essential for nanoscale modeling. Together, they enable semiclassical models like DD, EB, or hydrodynamic (HD) to account for phenomena such as tunneling, quantum confinement, and band mixing. This synergy is particularly important in devices like FinFETs, SOI MOSFETs, and heterostructures, where a combination of bulk material properties and detailed quantum corrections is essential for accurate transport simulations.

6.3.8 COMPARATIVE STUDY OF QUANTUM TRANSPORT MODELS IN FET DEVICE ENGINEERING

The choice of quantum modeling approaches in FET device engineering is essential for enhancing performance, predicting behavior, and advancing technology in devices such as MOSFETs, TFETs, HEMTs, double gate, FinFETs, and nanowire architectures. Each model has distinct applications and strengths that cater to specific device characteristics and operational challenges.

Here's a comprehensive Table 6.1 summarizing the transport models, categorized as *Classical*, *Semiclassical*, or *Quantum*, along with their *assumptions*, *applications*, and *limitations*:

TABLE 6.1
Comparative Overview of Classical to Semiclassical Models Discussed Above

Model	Type	Assumptions	Applications	Limitations
Drift-diffusion (DD)	Classical	Near equilibrium; negligible quantum effects; constant mobility	Bulk semiconductors, low-field FETs	Fails at nanoscale or high fields where quantum effects dominate
Hydrodynamic (HD)	Classical	Energy and momentum conservation; drift dominates over diffusion	High-speed devices, hot electron effects	Inaccurate for quantum-confined systems; computationally demanding
Energy balance (EB)	Semiclassical	Electron temperature; energy flux conservation	High-field transport in power devices, advanced FETs	Assumes local equilibrium for energy; less accurate for ballistic transport
Van Dort model	Semiclassical	Includes quantum confinement as a correction in MOS structures	Quantum capacitance in MOSFETs, nanostructures	Limited to narrow confinement corrections; lacks full quantum treatment

(*Continued*)

TABLE 6.1 (*Continued*)
Comparative Overview of Classical to Semiclassical Models Discussed Above

Model	Type	Assumptions	Applications	Limitations
Schrödinger–Poisson (SP)	Semiclassical	Solves quantum states with potential self-consistently	Quantum wells, 2D materials, nanoscale transistors	Computationally expensive; doesn't consider scattering
Quantum drift-diffusion (QDD)	Semiclassical	Quantum correction to DD; incorporates tunneling and confinement effects	Nanoscale MOSFETs, tunnel FETs	Limited accuracy for systems with significant quantum coherence or ballistic effects
Density gradient (DG)	Semiclassical	Quantum effects approximated by density gradients	Quantum corrections in nanoscale devices	Less accurate for strongly confined systems; lacks direct solution to Schrödinger's equation
Quantum hydrodynamic (QHD)	Semiclassical	Extends HD with quantum pressure and wave-packet dynamics	Quantum plasmas, nanoscale high-speed devices	Highly complex; requires accurate quantum closure relations
Quantum energy transport (QET)	Semiclassical	Energy flux conservation in quantum regime; coherence effects included	Advanced nanoscale device analysis, plasmonics	Computationally challenging; relies on approximate scattering models
Monte Carlo simulations	Semiclassical/ quantum	Tracks individual particle trajectories; considers scattering	Statistical transport, GaN HEMTs, avalanche breakdown	Requires many particles for accuracy; computationally intensive

6.4 ADVANCED QUANTUM MECHANICAL TECHNIQUES FOR SEMICONDUCTOR DEVICE ANALYSIS

The previous section, *Quantum Corrections to Classical Models,* involves applying quantum mechanical principles to improve or correct classical transport models (Schrödinger–Poisson, QHD, QDD, etc.). The above stated Quantum Corrections to Classical Models integrate quantum effects like tunneling, confinement, or quantized energy levels into classical frameworks. They use simplified approximations to handle quantum phenomena without fully abandoning the classical perspective. These approaches are computationally less intensive and provide insight into nanoscale device behavior while maintaining some classical assumptions. On the contrary, advanced quantum techniques (e.g., variational theory, WKB approximation, and perturbation theory) are sophisticated quantum methods that deal directly with the underlying physics of materials, particularly where approximations or perturbations to solvable conditions are necessary. For instance, WKB approximation aids in analyzing quantum tunneling problems. Perturbation theory applies to systems with slight deviations from exactly solvable scenarios.

These techniques are material-level but help understand foundational physics that transition smoothly into comprehensive quantum treatments such as Quantum Monte Carlo, Wigner–Boltzmann, and direct solutions to the N-body Schrödinger equation, etc. These methods discard classical simplifications and solve quantum systems directly, accounting for many-body interactions and complex dynamics.

They are computationally intense but essential for understanding phenomena that simpler models cannot capture, such as strong quantum coherence or correlated particle effects.

6.4.1 EVOLUTION FROM SEMICLASSICAL TO QUANTUM MODELS

As device sizes shrink, *semiclassical models* introduce quantum statistics (Fermi–Dirac) while still relying on classical trajectories. They account for scattering events but begin incorporating quantum effects like the Pauli exclusion principle [109]. *Quantum models* fully embrace wave-particle duality, describing particles with wavefunctions and focusing on phenomena like quantum tunneling, quantized energy levels, and probabilistic transport. These models are essential for nanoscale devices (below 10 nm), where quantum mechanics dominates, while semiclassical approaches bridge the gap for devices in the mesoscale (10–100 nm), combining both classical and quantum principles.

In FETs, *semiclassical transport models* use quantum mechanics to define the band structure (from which the electron's energy and momentum relationships are derived), but treat the motion of electrons in the electric field classically [110]. The *BTE* is commonly employed, often with corrections to include quantum effects like tunneling and scattering. These corrections emerge from quantum mechanical concepts but maintain the simplicity of a classical transport framework.

For instance, when we want to calculate stationary states and energy eigenvalues, we have a few handy techniques in our toolkit: *Perturbation Theory* was developed initially by Paul Dirac and others, perturbation theory became essential for analyzing quantum systems where the Hamiltonian can be broken into a solvable part plus a small perturbation [111]. *Variational Method* got formalized in quantum mechanics in the 1920s–1930s): While the variational principle dates back to classical mechanics, it was applied to quantum mechanics in the 1920s and 1930s to estimate the ground state energy of systems, by utilizing trial wavefunctions to minimize energy [112]. Named after Wentzel, Kramers, and Brillouin, *WKB approximation* method was introduced in the same year as the Schrödinger equation. It was developed to address problems with slowly varying potentials, connecting classical and quantum descriptions [113].

While not transport models themselves, variational theory, perturbation theory, and the WKB approximation provide foundational tools for solving quantum mechanical equations that underpin transport modeling. These methods are particularly valuable for understanding quantum states and energy levels in confined structures (e.g., quantum wells, nanostructures), approximating solutions in systems where exact analytical methods are intractable, such as in devices with small potential perturbations or nonuniform fields, analyzing quantum tunneling effects, crucial for understanding tunneling FETs (TFETs) or RTDs. For instance, they help refine the calculation of wavefunctions, effective masses, and tunneling probabilities, which are essential for integrating quantum effects into DD, DG, or NEGF models. Thus, they form the theoretical backbone for transitioning from classical to quantum descriptions in nanoscale device simulations.

6.4.2 VARIATIONAL METHOD

Let us begin with the *variational method*, a powerful technique used to approximate the ground state energy of quantum systems. The underlying principle of this method is that the expectation value of energy calculated using any trial wavefunction will always be greater than or equal to the true ground state energy. By systematically adjusting the parameters of the trial wavefunction, physicists can derive increasingly accurate estimates for the ground state energy. This method is particularly advantageous when exact solutions are unattainable, making it applicable across a wide range of complex systems. Furthermore, the variational method is relatively straightforward to implement, especially when a reasonable trial wavefunction can be proposed.

6.4.2.1 Evolution of the Variational Method

The variational method has evolved significantly over time, from a rudimentary guessing approach to a more sophisticated analytical technique that can be applied to complex quantum systems. Initially, it was applied in basic systems like the hydrogen atom and simple harmonic oscillator. As computational tools have advanced, the variational method has become a foundational tool in quantum mechanics, finding application in areas such as atomic, molecular, and solid-state physics.

The original approach involved guessing the form of the wave function and then using basic calculus to minimize the energy. This evolved into the development of more complex trial wavefunctions that could better approximate the ground state. The introduction of numerical techniques and computers allowed for more complex systems to be handled, making the variational method a staple in computational quantum mechanics.

6.4.2.2 Assumptions in the Variational Method

There are a few key assumptions behind the variational method. One of the most fundamental is that the chosen trial wavefunction must have an adjustable parameter, which can be varied to minimize the energy. This parameter controls the “shape” of the wave function, and by varying it, the method optimizes the approximation of the ground state energy.

Another assumption is that the Hamiltonian of the system is well-known and can be expressed in a form where the expectation value can be calculated. This method also assumes that the trial wavefunction is normalized, which simplifies the calculation of the energy expectation value.

Importantly, the trial wavefunction must be close enough to the true ground state wavefunction to yield a useful approximation. However, the method guarantees that the estimated energy will always be an upper bound to the true ground state energy, making it a reliable tool in many situations.

6.4.2.3 Analytical Expression of the Variational Method

The central idea of the variational method is to guess a wave function that depends on an adjustable parameter. For instance, let's consider a particle in a potential described by the Hamiltonian

$$H = \frac{p^2}{2m} + V(r) \tag{6.53}$$

where p is the momentum operator, m is the mass of the particle, and $V(r)$ is the potential energy.

To approximate the ground state energy, we first choose a trial wavefunction $|\psi(\alpha)\rangle$ where α is a parameter that can be varied to minimize the energy expectation value. The expectation value of the Hamiltonian$\langle H\rangle$ is given by [114]

$$E(\alpha) = \frac{\langle\psi(\alpha)|H|\psi(\alpha)\rangle}{\langle\psi(\alpha)|\psi(\alpha)\rangle} \tag{6.54}$$

The idea is to minimize $E(\alpha)$ by varying α, thus finding the best possible approximation to the ground state energy.

For a simple example, consider a particle restricted to one dimension and confined in a potential well. We can start by guessing a family of normalized Gaussian wavefunctions

$$|\psi(\alpha) >= (\alpha/\pi)^{1/4} e^{-\alpha x^2/2} \tag{6.55}$$

By calculating the expectation value of the Hamiltonian $\langle\psi(\alpha)|H|\psi(\alpha)\rangle$, differentiating with respect to α, and finding the minimum, we can estimate the ground state energy.

This method works exceptionally well for potentials like the simple harmonic oscillator, where the variational guess can lead to the exact solution. However, for other potentials, such as the attractive delta-function potential, the approximation might only be off by lower value, even which may still quite good given the simplicity of the method.

6.4.2.4 Variational Method Application in Field Effect Transistor (FET) Modeling

In the context of FETs, particularly at the nanoscale where quantum effects dominate, modeling the electronic properties and transport mechanisms becomes essential for accurate device performance prediction. Here, we can use a variational approach to model and estimate certain parameters, such as carrier energy states in confined structures, without solving complex differential equations directly.

We start by considering the quantum confinement of carriers (electrons or holes) along the z-axis in the triangular potential well created by the gate voltage. This potential confines electrons to a narrow inversion layer at the semiconductor–oxide interface.

The variational method allows us to estimate the ground state energy by choosing an appropriate trial wave function with a free parameter. By minimizing the expectation value of the energy, we can derive an expression for the energy subbands in the inversion layer of the MOSFET.

6.4.2.4.1 Step 1: Triangular Quantum Well Potential

In an n-channel MOSFET, the electric field F generated by the gate voltage forms a triangular potential well at the oxide–semiconductor interface. The potential energy as a function of the distance z from the interface is approximated as

$$V(z) = eFz \text{ for } z > 0 \tag{6.56}$$

Here, F is the electric field, and e is the electronic charge.

6.4.2.4.2 Step 2: Variational Trial Wavefunction

To apply the variational method, we guess a trial wavefunction that is physically reasonable for this system. Since the potential resembles a triangular well, the ground state wavefunction should be localized near $z = 0$ and decay as z increases. A common choice for a trial wavefunction in this scenario is [115]

$$\psi(z) = Aze^{-\alpha z} \tag{6.57}$$

where A is a normalization constant and α is the variational parameter that we will optimize to minimize the energy.

The form of this wavefunction is chosen because: It satisfies the boundary condition $\psi(0) = 0$, reflecting the fact that the wavefunction disappears at the semiconductor–oxide interface, and it decays exponentially for large z, which is consistent with the confining nature of the triangular potential.

6.4.2.4.3 Step 3: Normalization of the Trial Wavefunction

The trial wavefunction must be normalized, meaning

$$\int_0^\infty |\psi(z)|^2 \, dz = 1 \tag{6.58}$$

Substituting the trial wavefunction $\psi(z)$

$$A^2 \int_0^\infty z^2 e^{-2\alpha z} \, dz = 1 \tag{6.59}$$

The integral can be evaluated by standard procedure as

$$\int_0^{\infty} z^2 e^{-2\alpha z}\, dz = \frac{1}{(2\alpha)^3} \tag{6.60}$$

Thus, the normalization constant A is

$$A = \sqrt{8\alpha^3} \tag{6.61}$$

6.4.2.4.4 Step 4: Expectation Value of the Energy

The variational method involves minimizing the expectation value of the Hamiltonian, which consists of the kinetic and potential energy terms. The Hamiltonian is

$$H = -\frac{\hbar^2}{2m*}\frac{d^2}{dz^2} + eFz \tag{6.62}$$

where $m*$ is the electron effective mass.

The expectation value of the energy is

$$E(\alpha) = \langle \psi | H | \psi \rangle = \langle \psi | T | \psi \rangle + \langle \psi | V | \psi \rangle \tag{6.63}$$

T: kinetic energy operator, V: potential energy operator.

The kinetic energy expectation value is given by

$$\langle T \rangle = -\frac{\hbar^2}{2m*}\int_0^{\infty} \psi(z)\frac{d^2}{dz^2}\psi(z)\, dz \tag{6.64}$$

Substituting the trial wavefunction $\psi(z)$

$$\psi(z) = Aze^{-\alpha z} \tag{6.65}$$

$$\frac{d}{dz}\psi(z) = A(e^{-\alpha z} - \alpha z e^{-\alpha z}) \tag{6.66}$$

$$\frac{d^2}{dz^2}\psi(z) = A(-2\alpha e^{-\alpha z} - \alpha^2 z e^{-\alpha z}) \tag{6.67}$$

Evaluating the integral gives

$$\langle T \rangle = \frac{\hbar^2\alpha^2}{2m*} \tag{6.68}$$

The potential energy expectation value is

$$\langle V \rangle = \int_0^{\infty} \psi(z) eFz \psi(z)\, dz = A^2 eF \int_0^{\infty} z^3 e -^{2\alpha z}\, dz \tag{6.69}$$

Evaluating this integral gives

$$\langle V \rangle = \frac{3eF}{4\alpha} \tag{6.70}$$

6.4.2.4.5 Step 5: Total Energy Expectation Value

The total energy expectation value is the sum of the kinetic and potential energy terms:

$$E(\alpha) = \frac{\hbar^2\alpha^2}{2m*} + \frac{3eF}{4\alpha} \tag{6.71}$$

6.4.2.4.6 Step 6: Minimization of the Energy

To find the most favorable value of the variational parameter α, we need to minimize the energy E(α) with respect to α.

$$\frac{dE}{d\alpha} = \frac{\hbar^2\alpha}{m*} - \frac{3eF}{4\alpha^2} = 0 \tag{6.72}$$

Solving for α, we get

$$\alpha = \left(\frac{3eFm*}{4\hbar^2}\right)^{1/3} \tag{6.73}$$

6.4.2.4.7 Step 7: Subband Energy

Finally, substituting the optimal α back into the expression for the total energy gives the energy of the ground subband:

$$E_0 \propto \left(eF\hbar^2\right)^{2/3} m*^{-1/3} \tag{6.74}$$

Thus, using the variational method, we derived an approximate expression for the ground state energy (the lowest subband energy) in the inversion layer of a MOSFET. The energy subbands arise due to the quantum confinement of electrons in the triangular potential well formed by the gate electric field. The variational method provides a good approximation to the subband energies, which are essential for understanding charge transport in MOSFETs at the nanoscale level.

6.4.2.5 Limitations of Variational Method

Variational methods provide a robust framework for modeling semiclassical FETs, but there are a few key challenges:

- Variational methods rely heavily on trial wave functions. Imagine you're trying to model a complex system but only have a rough guess of what its true nature is. If that guess (the trial function) isn't accurate, the results will be far off. This is especially critical in semiconductor devices, where precision is everything.

- Semiclassical FETs often show nonlinear behaviors due to factors like strong electric fields. Variational methods might oversimplify this by not capturing all nonlinearities, which can lead to inaccuracies.
- FETs are getting more intricate as technology shrinks. Now, imagine trying to use variational principles to model this. You would need to account for every bend and curve of the structure.
- While variational methods aim for approximation, the reality is that optimizing multiple parameters in complex systems takes a lot of computational power.
- Quantum effects, especially in nanoscale devices, are critical. Variational methods might struggle to fully incorporate phenomena like tunneling or resonance, which are crucial for understanding device performance.

6.4.3 PERTURBATION THEORY

Next, we turn to *perturbation theory*, which is designed to analyze quantum systems that can be expressed as small deviations from a known, exactly solvable Hamiltonian. This technique allows for the calculation of corrections to energy levels and wavefunctions resulting from the introduction of a small perturbation. Perturbation theory is particularly effective in the context of weak interactions, commonly encountered in atomic and molecular physics. However, it is essential that the perturbation remains small; significant deviations can lead to inaccurate results and render the method ineffective [116].

6.4.3.1 Evolution of Perturbation Theory

Perturbation theory originated in classical mechanics, where it was used to solve problems involving small deviations from an idealized system, such as planetary orbits. In quantum mechanics, Erwin Schrödinger applied perturbation theory to approximate solutions for systems under small external influences. This method became foundational in atomic and solid-state physics [117]. Later developments, including Richard Feynman's diagrammatic methods, expanded perturbation theory's reach into fields like quantum electrodynamics [118].

6.4.3.2 Assumptions of Perturbation Theory

In the context of *semiclassical modeling* for *FETs*, perturbation theory plays a significant role.

In FETs, the electron dynamics in a periodic lattice (unperturbed system) are modified by external fields (perturbations). Perturbation theory assumes that these *external fields are small*, allowing for the corrections to be systematically calculated.

For small electric fields, carrier mobility and drift velocity are assumed to *respond linearly* to the field, $vd = \mu E$. This holds for low fields but begins to fail as fields grow stronger.

Electrons are modeled as wave packets in a crystal lattice. Perturbations like electric fields modify their position and momentum according to classical mechanics. This assumption works well for low-energy systems.

Perturbative techniques treat electron scattering events as independent and small, separating *elastic* (no energy change) and *inelastic* (energy exchange) scattering.

The model assumes that the electron's *band structure is known* and remains valid with minor corrections, enabling perturbative methods to calculate energy level changes.

6.4.3.3 Analytical Expression of Perturbation Theory

Here's how it works: perturbation theory takes a complicated quantum system and simplifies it by breaking it down into a basic system that we already understand, plus a small perturbation. The key idea is that if this perturbation is minor, the overall behavior of the system won't stray too far from the simpler, unperturbed version. The system is divided into two parts [119]:

1. The *unperturbed Hamiltonian* (H_0), representing the system we can solve exactly.
2. The *perturbing Hamiltonian* (H'), representing the small deviation from the unperturbed system.

Mathematically, the total Hamiltonian is written as

$$H = H_0 + \lambda H' \tag{6.75}$$

where λ is a small parameter that controls the strength of the perturbation. The goal of perturbation theory is to calculate the corrections to the energy and wavefunctions in a systematic way, as a power series in λ.

In time-independent perturbation theory, the system's Hamiltonian does not explicitly depend on time. The solution to the problem begins with the unperturbed system's known energy eigenstates, $E_n^{(0)}$, and unperturbed wavefunctions, $\psi_n^{(0)}$. The task is to calculate how these quantities change due to the perturbation H'.

The *first-order correction* to the energy is given by

$$E_n^{(1)} = \left\langle \psi_n^{(0)} \middle| H' \middle| \psi_n^{(0)} \right\rangle \tag{6.76}$$

Higher-order corrections can also be calculated, such as the second-order energy correction, which accounts for the interactions between the perturbed state and all other states.

In time-dependent perturbation theory, the perturbation varies with time, and this framework is used to study processes such as atomic transitions induced by an external electromagnetic field. For instance, an atom absorbing or emitting a photon is described using this formalism. The theory helps calculate transition probabilities between different quantum states, giving rise to important phenomena such as spontaneous emission and stimulated absorption in quantum optics.

6.4.3.4 Perturbation Theory Application in Field Effect Transistor (FET) Modeling

Let's go through an example where perturbation theory is applied to a MOSFET. Specifically, we will use perturbation theory to model corrections to the energy subbands in the inversion layer caused by a weak additional electric field.

Consider an n-channel MOSFET, where the inversion layer forms at the semiconductor–oxide interface under the influence of a strong electric field F_0 from the gate. The electrons are confined in a triangular potential well due to this electric field, and the unperturbed Hamiltonian can be solved as in the previous example. Now, let's assume there is a small additional electric field F_1 superimposed on F_0, which acts as a perturbation. The unperturbed energy E_0 corresponds to the energy of the electron in the triangular well formed by the strong electric field F_0. The first-order correction E_1 accounts for the effect of the small additional electric field F_1. This correction shifts the energy levels slightly, as expected when a weak perturbing electric field is applied to the system.

6.4.3.4.1 Step 1: Unperturbed Hamiltonian

The unperturbed Hamiltonian corresponds to the system without the additional electric field F_1, i.e., the triangular potential well with the original electric field F_0:

$$H = -\frac{\hbar^2}{2m*}\frac{d^2}{dz^2} + eF_0 z \tag{6.77}$$

This Hamiltonian is solvable using standard methods, and we already know the ground state energy for the unperturbed system from the variational method:

$$E_0 = \left(\frac{eF\hbar^2}{m*^2}\right)^{2/3} \tag{6.78}$$

6.4.3.4.2 Step 2: Perturbation Term

Now, we introduce a small perturbation due to the additional electric field F_1. The perturbation Hamiltonian is

$$H' = eF_1 z \tag{6.79}$$

This is considered a small perturbation relative to the unperturbed potential $eF_0 z$.

6.4.3.4.3 Step 3: First-Order Energy Correction

In first-order perturbation theory, the energy correction to the ground state due to the perturbation is given by

$$E_1 = \left\langle \psi_0 \middle| H' \middle| \psi_0 \right\rangle \tag{6.80}$$

Parameters as defined above.

For the triangular well, we approximate the ground state wavefunction using a similar form as before:

$$\psi^0(z) = Aze^{-\alpha_0 z} \tag{6.81}$$

$$\alpha = \left(\frac{3eF_0m*}{4\hbar^2} \right)^{1/3} \tag{6.82}$$

Substituting this into the expression

$$E_1 = eF_1 \int_0^\infty \psi_0(z) z \psi_0(z)\, dz \tag{6.83}$$

With

$$\psi^0(z) = Aze^{-\alpha_0 z} \tag{6.84}$$

we get

$$E_1 = A^2 eF_1 \int_0^\infty z^3 e -^{2\alpha_0 z}\, dz \tag{6.85}$$

Evaluating the integral gives

$$E_1 = \frac{3eF_1}{4\alpha_0} \tag{6.86}$$

Substituting the expression for α_0, we get the first-order energy correction:

$$E_1 = \frac{3eF_1}{4\left(\frac{3eF_0m*}{4\hbar^2} \right)^{1/3}} \tag{6.87}$$

6.4.3.4.4 Step 4: Total Energy

The total energy, including the first-order correction, is

$$E_{\text{total}} = E_0 + E_1 \tag{6.88}$$

Substituting the values

$$E_{\text{total}} = \left(\frac{eF\hbar^2}{m*^2} \right)^{2/3} + \frac{3eF_1(4\hbar^2)^{1/3}}{4(3eF_0m*)^{1/3}} \tag{6.89}$$

By applying perturbation techniques, we calculated the initial correction to the energy levels within the inversion layer of a MOSFET, accounting for the influence of a minor supplementary electric field. This approach can be extended to other types of perturbations, such as strain in the crystal or variations in doping concentration, to obtain corrections to the energy levels in MOSFETs analytically. This method provides a systematic way to account for small deviations from idealized systems, which is crucial in accurately modeling the performance of MOSFETs in real-world conditions.

6.4.3.5 Limitations of Perturbation Theory

Let's discuss the technical discussion surrounding perturbation theory and its limitations in the context of *semiclassical FETs*, particularly when scaled down to nanoscale devices.

a. Perturbation theory excels when dealing with small perturbations to a known system. However, in semiclassical FETs, especially at *high fields or in highly doped regions*, the *interaction strength between carriers and the lattice becomes significant*.
b. Perturbation theory, designed for weak interactions and smooth potentials, doesn't properly account for this *quantum mechanical tunneling* or *discrete energy states* in confined systems. This leads to discrepancies between what the theory predicts (e.g., gradual changes in carrier velocity) and what actually happens (e.g., abrupt changes due to tunneling).
c. In nanowire or nanosheet FETs, *randomly distributed dopants* introduce significant variability in device behavior. When dopant atoms are randomly distributed, they introduce localized fields that strongly affect carrier transport. This results in *inhomogeneous behavior*—the transport characteristics differ from point to point in the device, making it challenging for perturbation-based models to accurately describe the device performance.
d. At the nanoscale, *ballistic transport*—where electrons move through the channel without scattering—becomes a dominant phenomenon. Classical and semiclassical models that rely on scattering assumptions begin to fail here. Moreover, *quantum interference* effects can play a significant role in these small dimensions. Perturbation theory, which assumes a gradual evolution of wavefunctions, doesn't naturally incorporate the *wave-like behavior of electrons* that is essential to understanding interference and ballistic transport in such small devices.
e. At low electric fields, the relationship between drift velocity and the electric field is linear, which fits within the assumptions of perturbation theory. However, at *high electric fields*, this relationship becomes nonlinear, with the drift velocity saturating due to effects like *intervalley scattering* (where electrons scatter between different conduction band valleys with varying effective masses). Perturbation theory fails to model this nonlinearity because it assumes small, linear responses to external perturbations. This leads to *inaccurate predictions* at high fields where nonlinear effects dominate the device's behavior.

All of these challenges demand more robust modeling techniques that go beyond perturbation theory. *Non-perturbative methods* or full *quantum transport models* (e.g., using the NEGF method) are often required to accurately model these complex behaviors, particularly as devices continue to shrink in size and operate at more extreme conditions.

6.4.4 WKB (WENTZEL–KRAMERS–BRILLOUIN) METHOD

Lastly, we examine the *WKB* (*Wentzel–Kramers–Brillouin*) *method*, a semiclassical approximation that addresses the Schrödinger equation in scenarios with slowly varying potentials. The WKB method is particularly useful for estimating energy levels and wavefunctions in systems where quantum tunneling is significant. By approximating the wavefunction as a rapidly oscillating function, the WKB method enables the analysis of higher energy states and facilitates the study of phenomena at turning points, where the potential undergoes rapid changes. While the matching of solutions across different regions can introduce some complexity, the insights gained from applying the WKB method are invaluable, especially in contexts where classical mechanics remains relevant [120].

It is particularly effective in dealing with problems where quantum systems have well-defined classical counterparts, such as particle tunneling, quantum oscillators, and wave propagation in varying potentials. The method is essential for studying quantum systems with slowly varying potentials or in regions where the particle's de Broglie wavelength changes smoothly.

The WKB approximation offers an intuitive bridge between classical and quantum mechanics by providing approximate solutions where the precise solution of the Schrödinger equation is hard or impossible to compute analytically.

6.4.4.1 Evolution of the WKB Approximation

The evolution of the WKB approximation can be traced back to the early 20th century, as part of the development of quantum mechanics:

- **Classical Beginnings (Pre-1920s)**: Before quantum mechanics, classical physics governed the understanding of wave propagation. The study of wave phenomena in optics, acoustics, and mechanics led to early mathematical formulations for handling varying potentials.
- **Early Quantum Mechanics (1926)**: After the formulation of the *Schrödinger equation* in 1926, scientists sought ways to apply it to complex systems. The exact solutions of the equation were limited to specific potentials like the harmonic oscillator or hydrogen atom. For more general cases, physicists needed approximations to describe quantum behavior.
- **WKB Emergence (1926–1927)**: In the same period, *Gregory Wentzel*, *Hendrik Kramers*, and *Leon Brillouin* independently developed a semiclassical method to approximate solutions to the Schrödinger equation in quantum mechanics, now known as the *WKB approximation*. The approach generalized earlier work by *Harold Jeffreys* (1923), who had applied similar ideas to wave propagation in other fields of physics [121].

- **Further Development (Post-1927)**: Over the decades, the WKB method has been extended and applied to a wide range of quantum and classical problems, from particle tunneling in quantum barriers to approximations in cosmology.

6.4.4.2 Assumptions of the WKB Approximation

The WKB approximation is based on several key theoretical assumptions:

- **Semiclassical Approximation**: The particle is treated semiclassically, meaning its motion is approximately classical, but quantum corrections are considered. The wavefunction behaves like a rapidly oscillating wave in regions where classical mechanics is valid, and the de Broglie wavelength is slowly varying.
- **Slowly Varying Potential**: The approximation assumes that the potential $V(x)$ varies slowly compared to the wavelength of the particle's wavefunction, such that dV/dx is small. This allows the wavefunction to be treated as locally plane wave-like, with a varying amplitude and phase.
- **Large Quantum Numbers**: The WKB approximation is most accurate when the quantum number associated with the system is large (e.g., high energy states), leading to a slowly varying potential. It breaks down for small quantum numbers or in regions where the potential changes abruptly.
- **Turning Points**: The WKB approximation is designed for regions where the particle's classical energy is larger than the potential energy, $E > V(x)$. However, special care is needed near turning points, where the particle's kinetic energy becomes zero, $E = V(x)$.

6.4.4.3 Analytical Expression of the WKB Approximation

The time-independent *Schrödinger equation* for a one-dimensional quantum system is given by

$$\frac{d^2\psi(x)}{dx^2} + \frac{2m}{\hbar^2}[E - V(x)]\psi(x) = 0 \tag{6.90}$$

where $\psi(x)$ is the wavefunction, E is the energy of the particle, $V(x)$ is the potential energy, m is the mass of the particle, $\hbar$ is the reduced Planck's constant.

The WKB approximation assumes a wavefunction of the form:

$$\psi(x) \approx A(x)e^{iS(x)/\hbar} \tag{6.91}$$

where $s(x)$ is the action, and $A(x)$ is the amplitude of the wavefunction. Substituting this into the Schrödinger equation and using the semiclassical approximation, we get a simplified form of the equation:

$$S'(x)^2 = 2m[E - V(x)] \tag{6.92}$$

This equation can be solved in two regions as depicted in Figure 6.4.

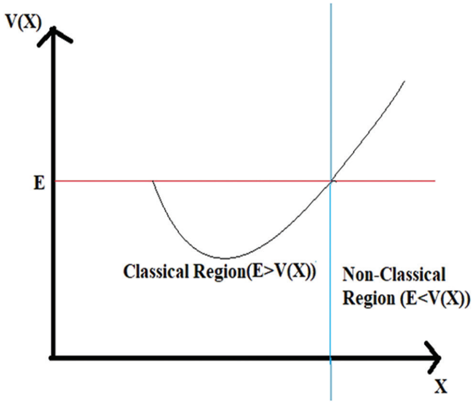

FIGURE 6.4 Pictorial representation of classically allowed region and classically forbidden region.

Classically Allowed Region $E > V(x)$ In this region, the particle can move freely, and the WKB solution is oscillatory. The wavefunction takes the form:

$$\psi(x) \approx \frac{C}{p(x)} \exp\left(\pm \frac{i}{\hbar} \int p(x')dx' \right) \tag{6.93}$$

where

$$p(x)^2 = 2m[E - V(x)] \tag{6.94}$$

is the classical momentum relation.

Classically Forbidden Region $E < V(x)$ In this region, the particle is classically forbidden from entering, but quantum mechanically it can *tunnel*. The solution in this region is exponential:

$$\psi(x) \approx \frac{C}{\sqrt{p(x)}} \exp\left(\mp \frac{i}{\hbar} \int p(x')dx' \right) \tag{6.95}$$

The key result of the WKB approximation is that it predicts both oscillatory behavior in classically allowed regions and exponential decay in classically forbidden regions, capturing the essence of quantum tunneling.

The WKB approximation finds applications in various areas of physics and engineering, one of the widely used is in calculating Quantum Tunneling in Semiconductor Devices

In semiconductor physics, the WKB approximation is used to model quantum tunneling of electrons through potential barriers, such as in *tunnel diodes* and *RTDs*. Tunneling current in MOSFETs and *tunneling field effect transistors* (*TFETs*) is often calculated using WKB-based models.

For example, the *tunneling probability* through a potential barrier $V(x)$ is given by

$$T(E) \approx \exp\left(-\frac{2}{\hbar} \int_{x_1}^{x_2} p(x)dx \right) \tag{6.96}$$

where x_1 and x_2 are the classical turning points, and $p(x)$ is the momentum of the particle.

The method is also applied to find approximate bound-state energies in quantum systems like potential wells. WKB provides insights into the transition between classical and quantum behavior, particularly in systems with high quantum numbers.

6.4.4.4 Modeling Tunneling Current in MOSFET Using WKB Approximation

In modern MOSFETs, as the oxide layer stuck between the gate and the channel becomes thinner (especially below 2–3 nm), electrons can tunnel through this thin oxide barrier, leading to gate leakage current. This tunneling effect can be modeled using the WKB approximation, which provides an estimate of the probability for an electron to tunnel through a potential barrier.

6.4.4.4.1 Step 1: Potential Barrier

The electron in the inversion layer of the MOSFET experiences a potential barrier formed by the gate oxide. The potential barrier height is approximately the energy difference between the conduction band edge in the silicon and the conduction band edge in the oxide. Let the potential barrier be represented as $V(z)$, where z is the distance perpendicular to the oxide layer.

The typical shape of the potential barrier for a FET is trapezoidal due to the electric field applied across the gate. We assume a simple triangular potential barrier for analytical ease. The potential can be expressed as

$$V(z) = V_0 - eFz \tag{6.97}$$

where V_0 is the barrier height and F is the electric field across the oxide.

6.4.4.4.2 Step 2: Schrödinger Equation and WKB Approximation

The time-independent Schrödinger equation for an electron of effective mass m∗ moving in the z-direction is

$$-\frac{\hbar^2}{2m*}\frac{d^2\psi(z)}{dz^2} + V(z)\psi(z) = E\psi(z) \tag{6.98}$$

Here, E is the energy of the electron.

The WKB approximation is valid when the potential changes slowly compared to the wavelength of the particle. Under the WKB approximation, the wave function $\psi(z)$ can be written as

$$\psi(x) \approx A(x)e^{\pm iS(x)/\hbar} \tag{6.99}$$

where $S(z)$ is the classical action and is related to the momentum $p(z)$ by

$$S(z) = \int p(z)\,dz, p(z) = \sqrt{2m*[E - V(z)]} \tag{6.100}$$

In the classically forbidden region, where $E < V(z)$, the momentum $p(z)$ becomes imaginary, leading to an exponentially decaying wavefunction:

$$\psi(z) \sim e^{-\int \kappa(z)dz} \tag{6.101}$$

$$\kappa(z) = \frac{\sqrt{2m^*[E - V(z)]}}{\hbar} \tag{6.102}$$

6.4.4.4.3 Step 3: Tunneling Probability Using WKB Approximation

Using above, the tunneling probability T as described above through a potential barrier in the WKB approximation

$$\langle T \rangle \sim \int_0^\infty \psi(z) \frac{d^2}{dz^2} \psi(z)\, dz \tag{6.103}$$

is given by

$$T \sim e^{-2} \int_{z_1}^{z_2} \kappa(z)\, dz \tag{6.104}$$

where z_1 and z_2 are the classical turning points, i.e., the points where $V(z_1) = V(z_2) = E$.

For the triangular potential barrier $V(z) = V_0 - eFz$ the turning points are

- $z_1 = 0$ (the start of the barrier at the gate/oxide interface),
- $z_2 = \frac{V_0 - E}{eF}$ (where the electron's energy equals the barrier height).

Thus, the tunneling probability becomes

$$T \sim e^{-2} \int_0^{\frac{V_0 - E}{eF}} \frac{\sqrt{2m^*[E - V_0 + eFz]}}{\hbar} dz \tag{6.105}$$

Evaluating the integral gives

$$T \sim e^{-4/3} \frac{\sqrt{2m^*}}{\hbar eF} (V_0 - E)^{3/2} \tag{6.106}$$

This is the tunneling probability for an electron with energy E to tunnel through the triangular potential barrier formed by the gate oxide.

6.4.4.4.4 Step 4: Tunneling Current Density

The tunneling current density J is related to the tunneling probability T and the number of electrons available to tunnel. The tunneling current density can be written as

$$J \sim \int_0^{V_0} T(E) f(E)\, dE \tag{6.107}$$

where *f*(*E*) is the distribution function for the electrons, typically modeled as a Fermi–Dirac distribution.

Substituting the expression for *T*(*E*) and using the fact that the tunneling probability decays rapidly with energy, we approximate the current density as

$$J \sim e^{-4/3\frac{\sqrt{2m*}}{\hbar eF}V_0{}^{3/2}} \tag{6.108}$$

In this example, the WKB approximation is used to model tunneling current in a MOSFET due to quantum mechanical tunneling through the gate oxide. The method provides a good analytical approximation for tunneling probability and current, which are critical for understanding and optimizing MOSFETs with thin gate oxides in modern devices. The WKB approximation is a powerful tool for modeling phenomena that involve quantum mechanical tunneling, especially in the presence of potential barriers that vary slowly over space.

Thus, the WKB approximation offers an intuitive bridge between classical and quantum mechanics by providing approximate solutions where the exact solution of the Schrödinger equation is difficult or impossible to compute analytically.

6.4.4.5 Limitations of WKB

This widely used semiclassical approximation technique in quantum mechanics is particularly valuable for modeling FETs. However, it has its limitations, especially when we venture into the nanoscale realm:

- First up, it tends to neglect quantum confinement effects at the interfaces of these tiny devices. As FET dimensions shrink, quantum effects become more pronounced and significantly impact carrier behavior. Unfortunately, the WKB method assumes a smooth potential, missing out on these critical phenomena essential for accurate device performance.
- Next, the method relies on the assumption of slowly varying potentials. But when things get tricky with rapidly changing potentials, the WKB approximation can stumble, leading to significant errors in predictions about device behavior under realistic conditions.
- Moreover, while it's great for calculating tunneling rates, the WKB method often struggles to accurately represent tunneling effects in nanoscale FETs. Its assumptions can leave the validity of its tunnel probability calculations ambiguous, making quantum tunneling—an important aspect of modern FET performance—hard to model accurately.
- The method also faces challenges capturing non-adiabatic effects. Since it's based on the adiabatic approximation, it assumes that state changes occur slowly, which isn't always the case in semiconductor devices at the nanoscale. Non-adiabatic effects, like Landau–Zener transitions, can significantly influence FET behavior, and the WKB method may not adequately account for these transitions.
- Lastly, boundary conditions are crucial for the accuracy of quantum mechanical models, yet the WKB method often struggles to provide precise

boundary conditions in complex geometries. This inadequacy can lead to inaccuracies in modeling carrier dynamics, particularly at the boundaries where transitions can heavily influence behavior.

While the WKB method is a valuable tool for semiclassical modeling of FETs, its limitations—such as neglecting quantum confinement, assuming slowly varying potentials, inaccuracies in tunneling calculations, struggles with non-adiabatic effects, and difficulties with boundary conditions—highlight the need for supplementary modeling approaches. As semiconductor technology advances, addressing these considerations becomes vital for tackling the complexities of increasingly sophisticated nanoscale devices.

6.4.5 Introduction to beyond Semiclassical Models

The *Schrödinger equation* is often hailed as a phenomenal breakthrough in physics, fundamentally reshaping our understanding of quantum mechanics. Formulated by Erwin Schrödinger in 1925, this equation describes how the quantum state changes over time. It allows for the calculation of wave functions, which provide vital information about the probabilities of finding particles in various states, ultimately leading to insights about their behavior. By capturing the dual wave-particle nature of matter, the Schrödinger equation laid the groundwork for much of modern physics and chemistry.

The *Schrödinger equation* governs the quantum behavior of carriers (electrons/holes), describing their wavefunctions and energy levels. When devices shrink to nanoscale, carriers exhibit wave-like behavior instead of being treated as classical particles. The *Poisson equation*, on the other hand, deals with the electrostatic potential in the device, linking the potential to the charge distribution. In this method, both equations are solved iteratively: Beginning with an initial estimate of the potential, the Schrödinger equation is employed to determine the distribution of carriers, which is subsequently utilized in the Poisson equation to refine the potential. This process continues until the results converge. *This self-consistent loop* is vital in modeling devices where quantum effects like electron confinement or tunneling dominate. For example, in *quantum wells*, electron energy levels become discrete, while in *nanoscale transistors* (like MOSFETs and FinFETs), quantum tunneling and subthreshold behaviors influence device performance. While being powerful, this approach can be computationally intensive, especially for 3D devices. Approximations like the effective mass model are often employed to make simulations feasible, though this may limit accuracy for certain materials.

The *BTE* bridges the semiclassical framework with quantum transport to understand how carriers move through a material, combining classical mechanics with quantum statistical distributions like the Fermi–Dirac distribution. The BTE assumes that carriers behave as point-like particles with well-defined positions and momenta but follow quantum statistical distributions (e.g., Fermi–Dirac distribution for fermions such as electrons).

It is to be noted that the Boltzmann equation and the BTE are closely related concepts but are not exactly the same. The *classical Boltzmann equation*, proposed by Ludwig Boltzmann in *1872*, lays the foundation for understanding the statistical behavior in a system out of equilibrium. In essence, it describes how particles like molecules in a gas spread out and collide, following classical physics principles [122]. These particles are treated as distinct entities that follow the *Maxwell–Boltzmann distribution*, meaning there's no limit on how many particles can occupy the same state. Collisions between them are governed by classical mechanics, with energy and momentum being conserved in the usual way. This framework works perfectly for large systems where quantum effects are negligible, like understanding how gases diffuse, heat transfers, or electric charge moves in a classical conductor. The general form of the Boltzmann equation considers how the distribution function of particles evolves over time due to their interactions, encapsulated mathematically as follows:

$$\frac{\partial f}{\partial t} + v \cdot \nabla f = Q(f) \tag{6.109}$$

Here, f is the distribution function, v represents particle velocities, and $Q(f)$ is the collision term accounting for particle interactions. On the other hand, the Q*BTE* came into play in the *20th century* to handle situations where quantum mechanics governs particle behavior [123]. Quantum particles, such as electrons in a semiconductor, follow different rules—namely, the *Fermi–Dirac* or *Bose–Einstein* statistics—depending on whether they are fermions or bosons. This means that fermions, like electrons, must obey the *Pauli exclusion principle*, preventing more than one particle from occupying the same quantum state. The quantum BTE incorporates wave-particle duality, tunneling, and quantum coherence, which are essential for describing transport in modern devices like *MOSFETs* or quantum dots. As a result, it provides a more nuanced picture of how particles move, especially at nanoscale dimensions where classical mechanics breaks down and quantum effects dominate. *BTE* provides a *kinetic description of particle transport* in non-equilibrium systems. This became necessary because:

- *Many-Body Systems* as semiconductors undergoing scattering, collisions, and interacting forces required a framework that could model statistical distributions of particles over time. BTE emerged to handle the *statistical distribution function* of particles, tracking their evolution in position and momentum space.
- While earlier methods often focused on equilibrium or near-equilibrium states, many real-world systems are *non-equilibrium* (e.g., heat conduction, current flow in semiconductors). The BTE evolved to describe how particles deviate from equilibrium and approach it over time, incorporating factors like external fields, collisions, and particle interactions.
- Classical and quantum transport phenomena, such as charge, mass, and heat transfer, involve *continuous interactions between particles.* This involves scattering, momentum relaxation, and diffusion, processes that need a statistical approach like BTE to model how particles move through a medium.
- The *QBTE* further refines this by considering *quantum mechanical scattering*, such as electron–electron interactions in semiconductors or quantum

interference effects in certain transport regimes. This made BTE a more *flexible and comprehensive model* for systems where classical and quantum mechanics overlap, particularly for materials science and semiconductor physics.

6.4.6 ASSUMPTIONS OF THE BOLTZMANN TRANSPORT EQUATION

The BTE operates under several key assumptions [124]:

- **Single-particle Distribution Function**: Carrier motion is described by the distribution function $f(r,k,t)$, which represents the probability of finding a carrier at a specific position *r*, with wave vector *k*, at time *t*.
- **Weak Quantum Effects**: The BTE neglects strong quantum effects like wavefunction coherence and quantum tunneling. It assumes that the de Broglie wavelength of carriers is much smaller than the characteristic length scales of the device (except in the direction of confinement).
- **Collision Integral (Scattering)**: Scattering events (with phonons, impurities, etc.) are treated using a collision integral $\Omega(f)$, which describes the rate of change in the distribution function due to these interactions. The scattering events are treated probabilistically.
- **External Forces**: The BTE accounts for external forces like electric fields *E* and magnetic fields *B*, which influence carrier motion through the *Lorentz force*.
- **Non-equilibrium Condition**: The BTE assumes that the system is out of equilibrium, where the carrier distribution is perturbed from the equilibrium distribution (such as Fermi–Dirac distribution). The equation describes how carriers relax back to equilibrium through scattering events.

6.4.6.1 Analytical Expressions of the Boltzmann Transport Equation

The BTE in its most general form is given as

$$\frac{\partial f(r,k,t)}{\partial t} + v_k \cdot \nabla_r f(r,k,t) + \frac{F}{\hbar} \cdot \nabla_k f(r,k,t) = \left(\frac{\partial f}{\partial t}\right)_{\text{Col}} \tag{6.110}$$

where $f(r,k,t)$ is the distribution function and $\partial f(r,k,t)/\partial t$ describes the rate of change of the distribution function with time.

The second term $v_k \cdot \nabla_r f(r,k,t)$ describes how carriers move through space, driven by their velocity v_k, related to the wave vector *k*.

The third term $\frac{F}{\hbar} \cdot \nabla_k f(r,k,t)$ represents how the external force (electric or magnetic field), and *F* influences carrier motion by altering their momentum *k*. $\hbar$ is the reduced Planck's constant.

$\left(\frac{\partial f}{\partial t}\right)_{\text{Col}}$ is the collision term (or collision integral), which accounts for changes in the distribution function due to scattering events. It also describes the probability that a carrier at a particular state (r,k,t) will scatter to a different state due to interactions with phonons, impurities, other electrons, etc.

The *solution of the QBTE* involves calculating the distribution function $f(r,k,t)$ in the presence of an electric field and scattering mechanisms.

In most practical applications, the BTE is too complex to solve exactly. Thus, it is often simplified using approximations. One of the most common simplifications of the BTE is the *relaxation time approximation* (*RTA*), which assumes that carriers relax toward an equilibrium distribution over a characteristic time τ, known as the *relaxation time*. Under the RTA, the collision term is simplified as

$$\left(\frac{\partial f}{\partial t}\right)_{\text{Col}} = -\frac{f(r,k,t) - f_0(k)}{\tau} \tag{6.111}$$

where $f_0(k)$ is the equilibrium Fermi–Dirac distribution function and τ is the average time between scattering events. This approximation simplifies the collision term by assuming that after each scattering event, the distribution function exponentially relaxes back toward the equilibrium state.

In macroscopic device modeling, the BTE is often simplified further to the *DD model* by assuming that carriers move due to both drift (under the influence of an electric field) and diffusion (due to concentration gradients).

In the context of a MOSFET, the key goal is to relate the electron distribution in the channel to measurable quantities like *current density J* and *charge density*. The current density in the channel is directly proportional to the integral of the distribution function over all momenta:

$$J = -q \int v_k f(r,k,t) \frac{d^3k}{(2\pi)^3} \tag{6.112}$$

6.4.6.2 Challenges from the BTE

The BTE is not purely classical; it incorporates essential quantum features like particle wave behavior and the Pauli exclusion principle. However, applying BTE to quantum systems presents challenges due to the inherent quantum nature of these systems. Quantum systems often operate far from equilibrium, where classical assumptions break down, and the BTE, relying on equilibrium-based Maxwell–Boltzmann statistics, may yield time-irreversible solutions that don't capture actual system dynamics.

Incorporating quantum effects into the BTE, especially in low-dimensional systems, introduces *non-Markovian* and *non-local behavior* [125]. Non-Markovian dynamics mean that the future state of the system depends on its history, violating the classical assumption that the future is independent of the past when conditioned on the present. In quantum systems, this memory effect is crucial as interactions with the environment can cause persistent correlations. Non-local behavior occurs when particle interactions are spread across large distances, a hallmark of quantum phenomena like entanglement and superposition. This challenges the conventional BTE, which assumes localized interactions, necessitating a rethinking of transport models in quantum contexts [126].

To overcome the challenges of integrating quantum effects into the BTE, researchers have devised several advanced methodologies and techniques. One of the key approaches is the development of sophisticated numerical methods tailored to quantum dynamics. For example, the Time-Evolving Matrix Product Operator (TEMPO) method offers a powerful framework for modeling non-Markovian dynamics in open quantum systems [127].

It is noteworthy to mention here that after the phenomenal Schrödinger equation, researchers were exploring kinetic theory more deeply, leading to the *Vlasov Equation* [128]. This equation describes the behavior of a plasma (or any collection of charged particles) in a non-collisional, electromagnetic field environment. It extends classical mechanics into plasma physics, but its real significance lies in the understanding of non-equilibrium systems without collisions—an early step toward handling non-equilibrium transport, which became critical in semiclassical and quantum modeling.

By 1928, the *Hartree Equation* introduced a mean-field approach for handling electron–electron interactions [129]. In this model, the behavior of each electron is influenced by the average effect of all other electrons in the system. This is a significant step toward incorporating many-body interactions in quantum mechanical systems without solving the full many-body Schrödinger equation, which is computationally prohibitive for large systems. The Hartree approach, while approximate, is widely used in quantum simulations of semiconductor devices to account for electron–electron repulsion in a more manageable way.

The Wigner method was introduced *in 1932 by Eugene Wigner* in his seminal paper. This work laid the foundation for what is now called the Wigner function, a phase-space formulation of quantum mechanics that extends classical statistical mechanics into the quantum realm. The Wigner method offers a unique approach to quantum transport by reformulating the density matrix into a phase-space representation through the Wigner function, a quasi-probability distribution that bridges classical and quantum mechanics. This method excels in capturing quantum effects such as tunneling, coherence, and interference, making it invaluable for analyzing non-equilibrium quantum transport in nanoscale devices like tunnel FETs, RTDs, and quantum wells. By solving the Wigner Transport Equation (WTE), it accounts for both quantum coherence and dissipative processes, providing insights that traditional models cannot. However, its quasi-probabilistic nature, where the Wigner function can exhibit negative values, complicates interpretation, and the computational demands for solving WTE in complex systems pose challenges. Despite these limitations, the Wigner method plays a crucial role in advancing the understanding and design of modern semiconductor devices where classical and semiclassical approaches fall short.

By the 1960s, the *NEGF* formalism provided a rigorous framework for describing quantum transport in non-equilibrium systems [130]. NEGF is used to model electron transport through devices where quantum effects like tunneling, wave coherence, and quantum confinement are critical. This model is essential for understanding transport in nanoscale devices, where classical models fail to capture the behavior of electrons [131]. Table 6.2 aims to provide a comparative overview of the models discussed above, and Figure 6.5 provides a visual representation of carrier transport models relevant to various active regions [132].

TABLE 6.2
Comparative Overview of Quantum Transport Models Mentioned Above

Model	Type	Assumptions	Applications	Limitations
Ballistic transport models	Quantum	Assumes carriers move without scattering	Sub-10 nm devices, nanowire FETs, TFETs	Fails in devices with significant scattering; ignores dissipative processes
Wigner transport equation (WTE)	Quantum	Treats quantum transport in phase space; includes tunneling and coherence	Tunneling devices, resonant tunneling diodes	Computationally expensive; difficult for large systems or complex geometries
Quantum Boltzmann Transport equation (QBTE)	Quantum	Extends classical BTE with quantum collision terms	Nanoscale transport, semiconductor lasers	Requires complex scattering integrals; not suited for strongly coherent systems
Non-equilibrium Green's function (NEGF)	Quantum	Fully quantum, includes coherence and scattering; solves transport via Green's functions	Nanoscale transistors, molecular electronics, quantum dots	Most computationally intensive; difficult to implement for large systems

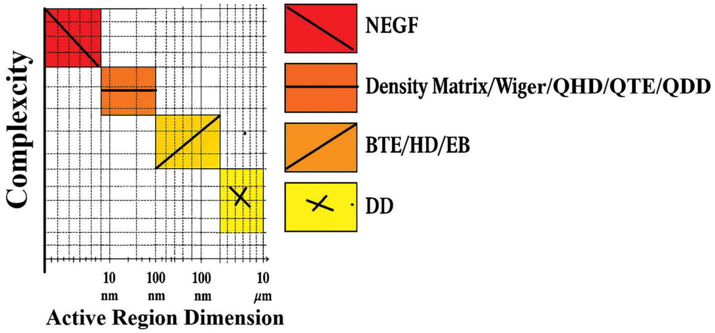

FIGURE 6.5 Pictorial representation of carrier transport models applicable in different active regions.

6.5 CONCLUSION

In conclusion, the transition from classical to semiclassical transport models in FETs is crucial for accurately capturing the dynamics of charge carriers in modern semiconductor devices. While classical models like the DD model and empirical approaches have been effective for larger devices, their limitations become evident as device dimensions shrink into the nanoscale regime, where quantum effects significantly influence carrier behavior. Quantum corrections through models such as the Schrödinger–Poisson self-consistent model and QDD models enable a more accurate description of charge transport phenomena, accounting for essential aspects like tunneling and quantum confinement. Advanced approaches, including QHD models and DG models, provide deeper insights into high-field transport and quantum statistical effects, making them particularly useful for emerging technologies like tunnel FETs (TFETs) and FinFETs. Additionally, the EMA and *k·p* method facilitate device modeling in complex material systems, allowing for greater accuracy in predicting performance under varying conditions. As semiconductor technology continues to evolve, the integration of quantum corrections becomes increasingly important to maintain the predictive power of simulation models. This chapter lays the groundwork for further exploration into approximate quantum solutions, namely variational theory, WKB approximation, and perturbation theory, which will enhance our understanding of the intricate interplay between quantum mechanics and charge transport in nanoscale devices. By bridging classical models with these advanced theoretical approaches, we prepare to tackle the challenges posed by the ongoing miniaturization of semiconductor components, ensuring that future innovations in device engineering are both feasible and grounded in robust theoretical frameworks. This progression underscores the necessity of adopting a multifaceted approach to device modeling that embraces both classical intuition and quantum mechanical rigor, ultimately guiding the next generation of semiconductor devices toward higher efficiency and performance.

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7 Scaling Capability Analysis of Junctionless Multi-Gate FETs

R. Ouchen, T. Berghout, F. Djeffal, and H. Ferhati

7.1 INTRODUCTION

The scaling of single-gate metal-oxide-semiconductor field-effect transistors (MOSFETs) transistor as had a profound impact on the miniaturization of semiconductor devices, driving the exponential growth in computing power and electronic functionality over the past several decades. However, as device dimensions continued to shrink, this scaling introduced a number of challenges that have influenced the trajectory of semiconductor miniaturization [1–5]. The continuous scaling of single-gate MOSFETs faced physical and material limitations, such as the thinning of the gate oxide and the increasing difficulty of reducing the channel length without compromising performance [6,7]. These scaling limits threatened the continuation of Moore's Law, which predicts the doubling of transistors on a chip approximately every 2 years [8,9]. Therefore, the optimization of gate structures in semiconductor devices has evolved significantly, with the evolution from the traditional single-gate to multi-gate FETs being a key strategy in overcoming the limitations of traditional MOSFET designs. This shift has been driven by the need for better electrostatic control, reduced leakage currents, and continued scaling as device dimensions shrink. By addressing the limitations of traditional MOSFETs, multi-gate FETs have enabled continued scaling, improved performance, and reduced power consumption in advanced semiconductor technologies. This evolution has been instrumental in sustaining the evolution of Moore's Law and driving the development of next-generation electronic structures. By utilizing multiple gates to control the current flow through the channel, multi-gate FETs offer superior electrostatic control, reduced short-channel effects (SCEs), and improved performance, enabling further miniaturization of semiconductor technology [6].

In a double-gate FET, the transistor features both gates that commend the channel from tow the top and bottom (or from opposite sides). These gates can be independently biased or connected to the same voltage source, depending on the desired operation [10]. The channel is typically a thin layer of semiconductor material sandwiched between the two gates, allowing both gates to influence the flow of charge carriers within the channel. Double-gate FETs are particularly practical in low-power applications where precise control of the channel is critical. They are also used in some memory devices and analog circuits where enhanced control over the transistor characteristics is needed.

DOI: 10.1201/9781003543923-7

Multi-gate FETs, including FinFETs and Gate-All-Around (GAA) FETs, extend the concept of double-gate (DG) FETs by adding more gates around the channel. This architecture can include three gates (tri-gate) or completely surround the channel (GAA) [11–16]. In a FinFET, the channel is shaped like a vertical fin, and the gate wraps around three sides of the fin, offering improved control over the channel compared to single- or double-gate structures. However, the gate in the GAA FETs completely surrounds the channel providing the most comprehensive control. The channel can be in the form of a nanowire or nanosheet, with the gate enveloping it entirely.

Multi-gate FETs are widely used in advanced processors, mobile devices, and other integrated circuits (ICs) where performance, power efficiency, and scaling are critical. They are the dominant transistor architecture in modern semiconductor manufacturing for technology nodes below 20 nm [15–19].

Another advanced class of transistors designed to overcome the limitations of traditional MOSFETs and provide better scalability, performance, and power efficiency is the Junctionless Multi-Gate Field-Effect Transistors (JLMG FETs) [20–22]. Unlike conventional FETs, junctionless FETs do not have p–n junctions between the channel and source/drain regions. Instead, the entire structure is uniformly doped, simplifying fabrication and enhancing control over SCEs. JLMG FETs represent a promising advancement in semiconductor technology, addressing many of the challenges faced by traditional single-gate FETs. By eliminating junctions and leveraging multi-gate architectures, these devices offer enhanced electrostatic control, reduced leakage currents, and improved scalability.

The aim of this chapter is to study key advancements in transistor structure design, focusing on the scaling capabilities and performance advantages of DG and GAA MOSFETs—areas that are pivotal in cutting-edge semiconductor research. Also, as semiconductor technology advances, these innovative structures are vital for continued miniaturization, reducing power consumption, and enhancing device speed, thus driving the development of next-generation semiconductor devices.

7.2 FROM SINGLE-GATE TO MULTI-GATE FETs

Because MOSFETs are fundamental components in the development of ICs, they play an important role in achieving high levels of flexibility and performance. The versatility of MOSFET devices extends across a large range of applications, from memory storage to portable calculators, making them indispensable in various fields. Therefore, a huge benefit is gained by rendering devices smaller, which increases the packing density and improved ratio functionality/area. This allows for more efficient use of space, resulting in improved performance and the ability to integrate more features within a smaller footprint.

7.2.1 The Era of Single-Gate FETs

In the early 1960s, the MOSFET was developed [8, 23–25]. It quickly became the backbone of digital electronics due to its simplicity, low power consumption, and scalability. The traditional MOSFET features a single gate that controls the current

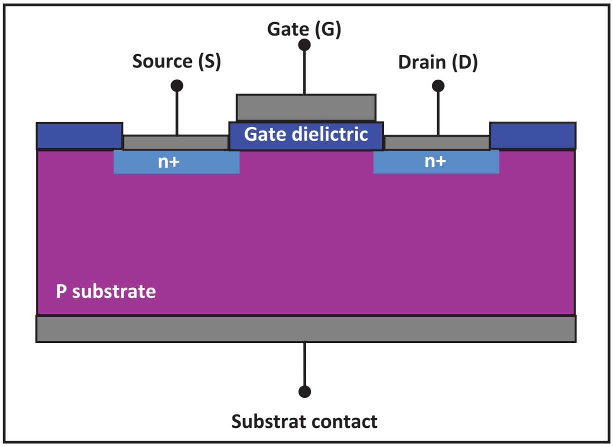

FIGURE 7.1 Schematic illustration of a typical MOSFET device.

between the both terminals by modulating the conductivity of a semiconductor channel as shown in (Figure 7.1). The single-gate MOSFET enabled the development of ICs, leading to the rapid growth of the semiconductor industry and the realization of Moore's Law [6,26–30]. Throughout the 1970s to the 1990s, the semiconductor industry focused on scaling down the dimensions of single-gate MOSFETs to increase transistor density and improve performance.

As MOSFETs were scaled below 1 µm, engineers began to encounter significant challenges, such as SCEs, where the control of the gate over the channel diminishes, leading to issues like leakage currents and threshold voltage instability [31,32]. To mitigate some of these challenges, the introduction of high-k dielectrics and metal gates in the late 1990s helped to reduce gate leakage and improve performance, but further scaling required more radical innovations [7].

7.2.2 DOUBLE-GATE STRUCTURES

In 1980s, the idea of using two gates to control the channel more effectively has been emerged as a theoretical solution to the scaling limitations of single-gate MOSFETs. So, DG FET structure is advanced architecture in the field of transistor design (Figure 7.2), and it is first key to enable continued scaling of semiconductor devices [33,34]. Those transistors promised better electrostatic control over the channel, reduced SCEs, and the potential for further miniaturization. A decade after, researchers developed experimental DG FETs, demonstrating that two gates could indeed provide better control over the channel, reducing leakage currents and improving drive strength.

7.2.2.1 Planar Double-Gate FET (DG FET)

The planar DG FET has two gates on opposite sides of a thin semiconductor channel, typically fabricated on a silicon-on-insulator (SOI) substrate [35]. The planar DG FET is analogous to the traditional bulk CMOS technology but with reduced

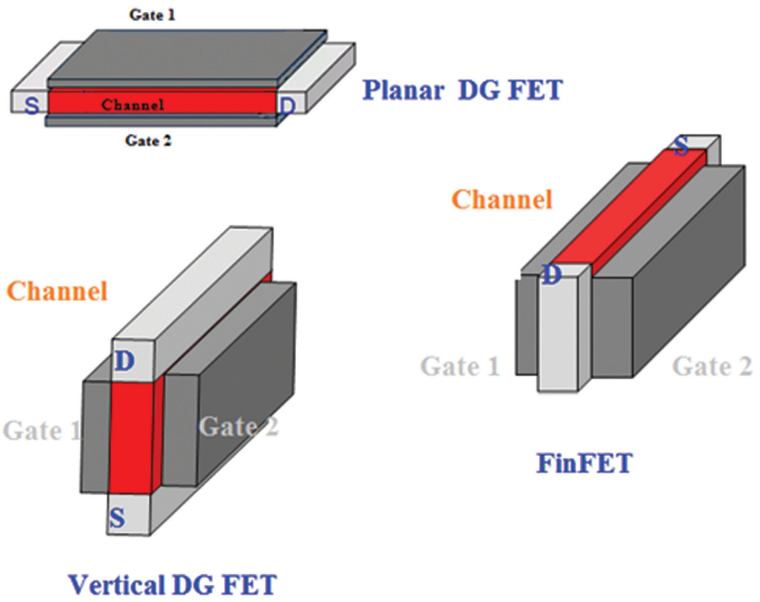

FIGURE 7.2 Schematic view of the (a) planar double-gate MOSFET, (b) the FinFET and (c) the vertical double-gate MOSFET. While the current flows in plane with the surface in (a) and (b), in (c) it flows perpendicular to it.

geometric issues (Figure 7.2), such as "corner effects" and "narrow width effects." Moreover, the planar DG design avoids the "crystal plane orientation uncertainty" problem that arises when device orientations differ. Another benefit of the planar DG FET is that the two gates can be easily biased independently, as they are fabricated in separate processing steps. Both gates control the channel simultaneously, providing enhanced control over the electrostatic potential in the channel. The planar DG FETs are suitable for low-power and high-performance logic circuits where planar integration is preferred.

7.2.2.2 Vertical Double-Gate FET

In the vertical DG FET, the channel is oriented vertically, with gates on opposite sides of the channel. This structure allows for a more compact layout compared to planar designs (Figure 7.2). The vertical orientation can lead to improved electrostatic control and is often used in power transistors or devices where vertical integration is beneficial. In power electronics and 3D ICs, vertical stacking is advantageous [36,37].

7.2.3 MULTI-GATE STRUCTURES

To enhance addressing undesirable effects, more new FET architecture, the Multi-Gate (MG) FET, has been proposed and studied [38,39]. In these devices, SCEs are more effectively controlled by the dimensions of the silicon and oxide layers, resulting in less noticeable subthreshold slope (SS) degradation. Notably, the ideal SS, assuming no short-channel degradation, is known to be 60 mV per decade [40].

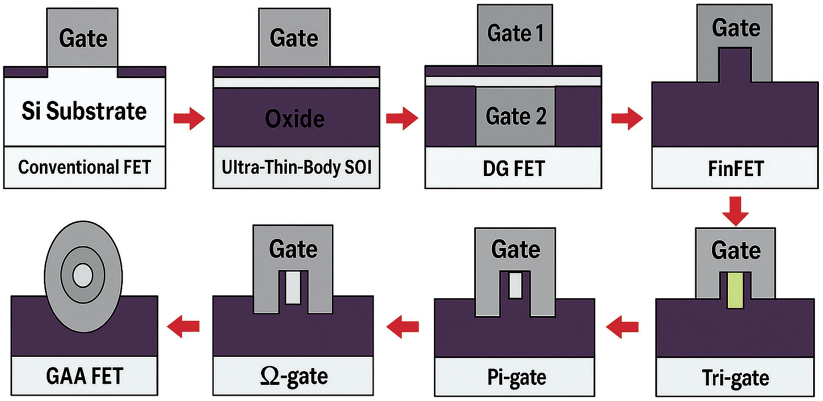

FIGURE 7.3 Multi-gate structures evolution. Image based on King Liu, 2012.

Figure 7.3 illustrates the evolution of MOSFET structures, including DG, tri-gate, pi-gate, omega-gate, and GAA designs. DG and tri-gate FinFETs are particularly popular because of their straightforward design and ease of fabrication. Although the GAA device was conceptualized before the FinFET, FinFETs were more practical for large-scale production.

7.2.3.1 FinFET (Fin Field-Effect Transistor)

In 1999, researchers at the University of California were introduced a new transistor structure, the FinFET (Fin Field-Effect Transistor) (Figure 7.2). The FinFET featured a thin, fin-like channel with a gate that wrapped around three sides of the fin [41]. They offered significantly improved commend over the channel in comparison to that of single- and DG MOSFETs. So, they reduced SCEs, leakage currents, and allowed for better scaling to smaller nodes. However, by the early 2000s, FinFETs began to be adopted by major semiconductor manufacturers. They became the standard transistor architecture for technology nodes at 22 nm and below. And, they are widely used in modern processors, mobile devices, and other advanced ICs, particularly in technology nodes of 14, 10, 7 nm, and beyond [42,43]. As technology nodes reached 7 and 5 nm, FinFETs began to face limitations in further scaling, prompting the semiconductor industry to explore GAA FETs for future nodes.

7.2.3.2 Tri-Gate FET

Another structure similar to the FinFET, the tri-gate FET also has a three-sided gate structure (Figure 7.3). However, the term “tri-gate” often refers to the specific implementation where the gate completely encloses the fin from three directions, sometimes with more emphasis on planar integration [44]. The gate’s comprehensive control over the channel reduces leakage currents and enhances drive strength, making it highly efficient for high-performance and low-power applications. They are used in high-speed processors and other ICs that require balanced performance and power efficiency [45].

7.2.3.3 Gate-All-Around (GAA) FETs

GAA FETs, where the gate fully surrounds the channel, were conceptualized as an evolution of MG FETs (Figure 7.3). Early prototypes in the 2000s demonstrated even greater control over the channel than FinFETs. GAA FETs evolved into two main variants: nanowire and nanosheet FETs. Nanowire GAA FETs feature a cylindrical channel surrounded by the gate, while nanosheet GAA FETs have a flat, ribbon-like channel surrounded by the gate [46,47].

GAA FETs provide the best electrostatic control among all FET structures, virtually eliminating SCEs and minimizing leakage currents. They are highly scalable and are seen as the future of transistor technology for nodes below 5 nm. Consequently, leading semiconductor companies like Samsung and TSMC have announced plans to use GAA FETs in their upcoming 3 and 2 nm processes, marking the next major transition in transistor architecture. Therefore, future of MG FETs may involve 3D integration, where multiple layers of transistors are stacked vertically to further increase transistor density and performance. And, the use of new materials, such as 2D materials (e.g., graphene) and high-mobility semiconductors, can enhance the performance of MG FETs.

In GAA FET structure, the channel can be in the form of a nanowire, nanosheet, or nanotube, with the gate wrapping around all sides. Nanowire GAA FET: Features a cylindrical nanowire channel surrounded by the gate [48,49]. It offers superior electrostatic control and high scalability. The second subtype is the nanosheet GAA FET; it uses a flat, ribbon-like channel surrounded by the gate and provides a larger effective channel width, leading to higher drive currents compared to nanowires. These two types are emerging as a key technology for nodes at 5 nm and smaller, with potential use in high-performance computing, AI, and other cutting-edge applications.

7.2.3.4 Surround-Gate Transistor (SGT)

The surround-gate transistor is a variant of the GAA FET where the gate fully encircles the channel (Figure 7.4), similar to the GAA structure but sometimes applied in different geometries or materials [50]. It offers maximal gate control over the channel, ideal for minimizing SCEs and enhancing device performance, widely used in advanced memory devices, high-speed processors, and applications requiring extreme miniaturization.

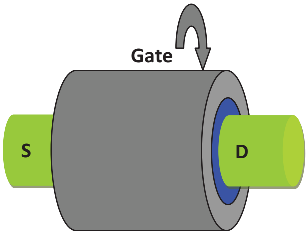

FIGURE 7.4 The surrounding gate MOSFET device.

7.2.3.5 Omega-Gate FET

The Omega-Gate FET has a gate that forms an omega (Ω) shape, wrapping around three sides of the channel [51]. It's a variant of the FinFET, with more extensive gate coverage (Figure 7.3). It provides superior control over the channel compared to traditional FinFETs, with reduced leakage and improved drive current. This kind of structure is appropriate for high-performance computing and ultralow-power purposes.

7.2.3.6 Pi-Gate FET

The Pi-Gate FET is a specialized structure where the gate forms a π-shape, covering more of the channel compared to standard MG designs (Figure 7.3). It offers enhanced electrostatic control and is designed for applications that demand even greater reduction in SCEs. Pi-Gate FETs are mainly used in experimental and cutting-edge semiconductor research for potential future [39].

7.3 JUNCTIONLESS MULTI-GATE FETs

7.3.1 Junctionless Transistors Design

In conventional MOSFETs, the source/drain parts are doped with opposite types of impurities (n-type or p-type) relative to the channel (Figure 7.5). A p–n junction forms between these regions and the channel, and the transistor operates by using the gate voltage to modulate the carrier concentration in the channel. Unlike traditional MOSFETs, where the channel, source, and drain are doped differently, a junctionless transistor features a uniformly doped semiconductor channel. The entire channel is either n-type or p-type, depending on the desired type of carrier (electrons or holes). As the name suggests, junctionless transistors do not have p–n junctions. This concept began to emerge in the late 1990s and early 2000s. Researchers theorized that eliminating the p–n junctions in transistors could simplify the manufacturing process and reduce some of the issues associated with traditional transistors. In a junctionless transistor, the entire channel is uniformly doped, and the transistor operates by depleting the charge carriers in the channel to turn off the current flow. This contrasts with conventional MOSFETs, where the gate modulates the carrier

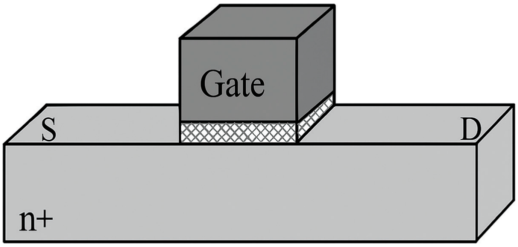

FIGURE 7.5 A 3D double-gate JL FinFET device.

density across a junction. In 2009, the first experimental demonstrations of junctionless transistors were reported by researchers led by Jean-Pierre Colinge at the Tyndall National Institute in Ireland. This was a major breakthrough, proving that junctionless transistors could function effectively and offer certain advantages over conventional transistors [52–54]. The initial junctionless transistors were fabricated using silicon nanowires, which allowed for precise control of the channel thickness and doping concentration. The nanowire structure also made it easier to achieve full depletion of the channel.

7.3.2 Basic Principle of Junctionless Transistors

The junctionless transistor operates primarily in depletion mode. When no voltage is applied to the gate, the channel is conductive, allowing current to flow. Applying a voltage to the gate depletes the carriers in the channel, reducing or stopping the current flow. Essentially, the gate voltage controls the degree of depletion in the uniformly doped channel. When the gate voltage is low or negative (for n-type junctionless transistors), the channel remains conductive and free charge flows between the drain and source terminals. When the gate voltage is increased (positive for n-type), it depletes the majority carriers in the channel, effectively "pinching off" the current flow, turning the transistor off. The absence of p–n junctions simplifies the doping process, as there is no need to create sharply defined regions with different doping types. This reduces manufacturing complexity, especially at nanoscale dimensions where precise junction formation becomes challenging. Additionally, the uniform doping profile makes junctionless transistors more scalable as device dimensions shrink, offering potential advantages in producing smaller, more densely packed transistors. The gate's ability to control the entire uniformly doped channel can reduce SCEs, such as drain-induced barrier lowering (DIBL) and threshold voltage roll-off, which are common in aggressively scaled traditional MOSFETs [55–58]. With better electrostatic control, junctionless transistors can exhibit lower leakage currents and higher on/off current ratios, improving overall device performance. However, achieving precise control over the threshold voltage in junctionless transistors can be challenging. The threshold voltage is greatly impacted by the device geometry and channel doping, requiring careful design to ensure consistent performance. There is often a trade-off between achieving low threshold voltages (for better performance) and maintaining sufficient depletion in the off-state to minimize leakage currents. So, despite their advantages, junctionless transistors are not yet widely adopted in commercial semiconductor manufacturing. They are primarily used in niche applications where their specific benefits outweigh the challenges, such as in certain low-power and high-reliability devices.

7.3.3 Evolution to Junctionless Multi-Gate FETs

The junctionless concept was naturally extended to MG FETs, where several gates are employed to better control the channel from different directions. MG structures, such as FinFETs and GAA FETs, were already known for their superior electrostatic

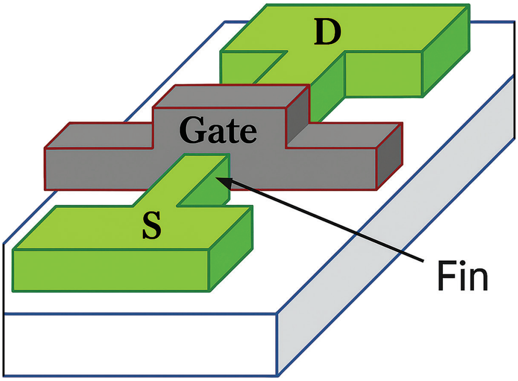

FIGURE 7.6 Junctionless FET longitudinal cross section [59].

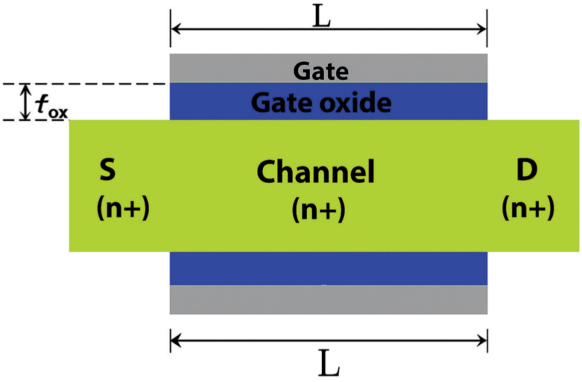

FIGURE 7.7 Two-dimensional GAA JL MOSFET cross-sectional views [62].

control, and combining these with the junctionless approach further enhanced performance. One of the first implementations was the junctionless FinFET (Figure 7.6) [59], where a fin-like channel is controlled by gates on three sides. This structure provided excellent electrostatic control, reduced SCEs, and simplified the fabrication process by eliminating the need for precise junction formation.

Similarly, the junctionless concept was applied to GAA FETs, where the gate surrounds the channel completely [22,60,61], offering even greater control and reducing leakage currents to near-zero levels (Figure 7.7) [62]. Therefore, combining the junctionless transistor concept with MG structures has led to a novel class of transistors that leverage the strengths of both approaches. A JLMG FET combines the uniform doping of the junctionless transistor with the superior electrostatic control of MG architectures. In this structure, the channel is uniformly doped, and the multiple gates work together to provide a stronger and more uniform electric field that can more precisely deplete the channel. This leads to better control over the on/off states of the transistor, reducing leakage currents and enhancing the on-state current.

Many structures have been introduced, in a junctionless FinFET, the channel takes the form of a thin fin, with gates placed on three sides. The gates deplete the uniformly doped fin to control the current, taking advantage of both the simplified fabrication of junctionless transistors and the strong electrostatic control of the FinFET design. In a junctionless GAA FET, the gate fully surrounds the channel, providing the ultimate level of control. This design minimizes SCEs even further, making it highly effective for nanoscale devices [63–65].

7.3.4 ADVANTAGES OF JUNCTIONLESS MULTI-GATE FET

JLMG FETs offer numerous advantages over traditional transistor designs, particularly in terms of simplified fabrication, enhanced control, improved scalability, and reduced variability. These benefits make them a strong candidate for future semiconductor technologies, especially as the industry continues to push the limits of miniaturization and performance. So, junctionless transistors eliminate the need for forming source/drain junctions, simplifying the doping process and reducing the complexity of the manufacturing process. Additionally, this approach allows for better scaling to smaller technology nodes, as it reduces the issues related to SCEs and threshold voltage variability. Moreover, it leads to an enhanced performance by offering low off-state leakage currents and high drive currents [5,63,64,65].

7.3.5 CHALLENGES AND LIMITATIONS

While JLMG FETs offer several advantages, they also face several challenges that need to be addressed for their successful implementation in advanced semiconductor applications. These challenges include threshold voltage control, process variability, SCEs, self-heating, scaling difficulties, manufacturing complexity, integration with existing technologies, and reliability concerns. Overcoming these challenges requires ongoing research and development, as well as advancements in materials, fabrication techniques, and design tools. Despite these challenges, the potential benefits of JLMG FETs make them a promising technology for the future of semiconductor devices, particularly as the industry continues to push the limits of miniaturization and performance. Their unique advantages, particularly in terms of simplified fabrication and improved performance, position them as a key technology in the continued evolution of electronic devices. The simplified structure and excellent control make these transistors candidates for use in emerging computing paradigms, such as neuromorphic computing (which mimics the human brain) and quantum computing.

7.3.6 JUNCTIONLESS GAA FET NUMERICAL SIMULATIONS

Numerical simulation of Junctionless GAA FETs is a powerful tool that provides accurate device modeling, enables design optimization, reduces development costs, and supports innovation. It helps in predicting device behavior, optimizing performance, and addressing scaling challenges. So, to model complex physical phenomena and provide valuable insights into the performance characteristics particularly in terms of power efficiency, switching speed, and scaling potential of the investigated

JL GAA FETs, simulations using ATLAS technology computer-aided design (TCAD) simulator were performed [66]. As shown in Figure 7.7, L is the gate length of the device channel, *R* is the radius ($R = 2.5$ nm), and SiO_2 is an interface layer with t_{ox} denoting its thickness ($t_{ox} = 1$ nm). These simulations are essential for understanding how the swing factor (SS) and off-state current (I_{OFF}) vary with different channel lengths (*L* from 10 to 60 nm). In this context, the device is considered with JL structure for which the channel region is considered n-type uniformly doped with concentration of $10^{19}/cm^3$. Simulating the impact of channel length (*L*) variation on the SS, I_{OFF}, and the I_{ON}/I_{OFF} current ratio is essential for understanding the behavior and performance of the model. These simulations show that the SS, which indicates the efficiency of the transistor switching from off to on state does not vary significantly with changes in channel length (Figure 7.8). Similarly, Figure 7.9 shows a consistent IOFF; I_{OFF} represents the small amount of current that flows when the transistor is in the off-state, An invariant SS indicates good control over the channel and consistent switching behavior. A consistent I_{OFF} current is an indicator of good device design, strong electrostatic control, and low static power consumption, but it does not guarantee that the I_{ON}/I_{OFF} ratio will remain invariant (Figure 7.10). The I_{ON}/I_{OFF} ratio can vary due to factors like leakage currents, threshold voltage shifts, and changes in device characteristics with scaling. Therefore, while invariant SS is a good sign of robust device design, additional considerations are needed to ensure stable I_{ON}/I_{OFF} ratio. Simulating these parameters is essential for designing next-generation transistors that meet the performance and efficiency requirements of modern electronics, including low-power, high-speed, and high-density applications.

In summary, when SS does not vary with channel length in Junctionless GAA FET simulations, it generally indicates robust device performance and effective electrostatic control, which are desirable traits for modern transistor designs. An invariant

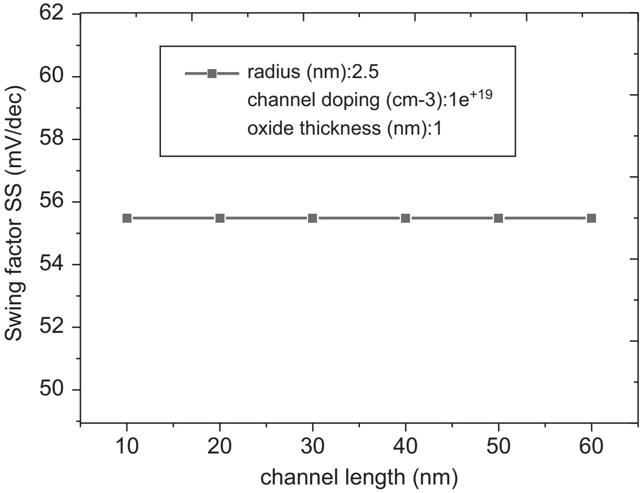

FIGURE 7.8 Swing factor (SS) versus channel length (*L*) with $R = 2, 5$ nm, $N_d = 10^{19}/cm^3$, and $t_{ox} = 1$ nm.

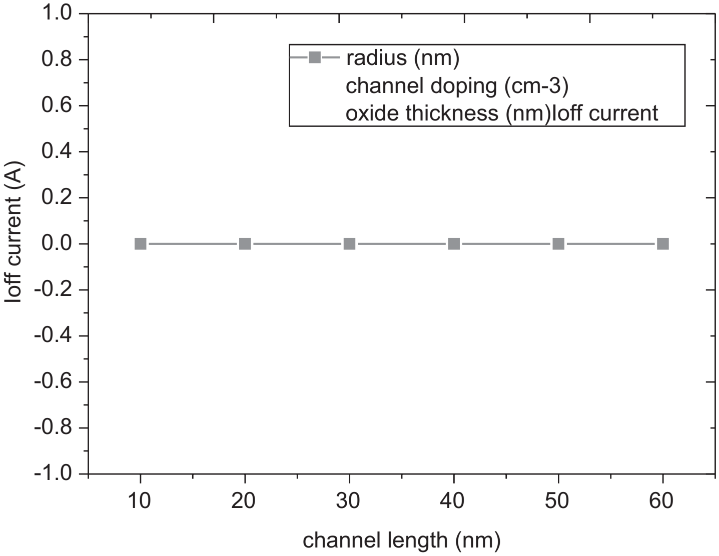

FIGURE 7.9 I_{OFF} versus channel length (L) with $R = 2, 5$ nm, $N_d = 10^{19}/\mathrm{cm}^3$, and $t_{\mathrm{ox}} = 1$ nm.

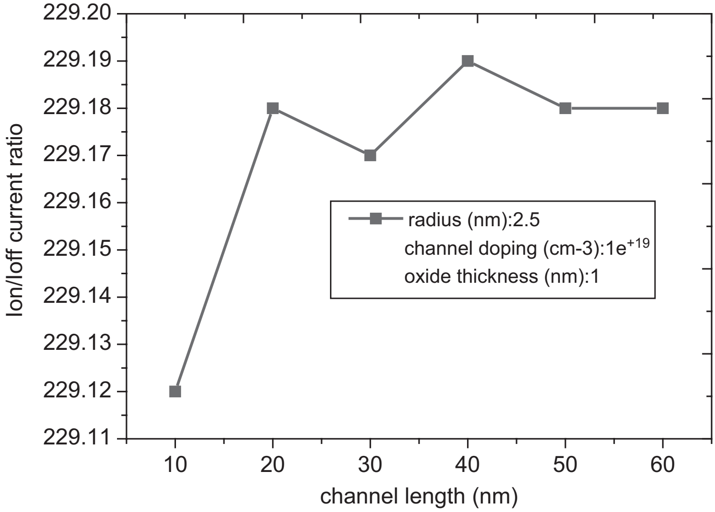

FIGURE 7.10 $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio versus channel length (L) with $R = 2, 5$ nm, $N_d = 10^{19}/\mathrm{cm}^3$, and $t_{\mathrm{ox}} = 1$ nm.

SS, I_{OFF}, and $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ current ratio across varying conditions signify a well-designed transistor that maintains its performance characteristics consistently. This is highly desirable in advanced semiconductor technology, where maintaining control over these parameters is essential for further scaling and integration of devices into modern electronic systems.

7.4 MACHINE LEARNING-ASSISTED DESIGN OF JUNCTIONLESS GAA FET

The dataset utilized in this study comprises 147 observations of Junctionless MG FETs, each characterized by variables including oxide permittivity, channel doping, oxide thickness, and channel radius. The OFF-sate current (I_{off}) is also recorded for each observation and categorized into three classes—Good, Medium, and Worst—based on predefined thresholds. This categorization is crucial for evaluating the scalability and performance of the devices.

To prepare the dataset for analysis, several steps were undertaken. First, the feature matrix, containing the previous four key variables, was normalized to a range of [0, 1] to ensure consistency across features. Subsequently, the dataset was balanced using the Synthetic Minority Over-sampling Technique (SMOTE) to address any class imbalance, resulting in a more equitable distribution of the class labels [67]. Feature importance was assessed using a decision tree model both before and after the balancing process [68]. This analysis provided insights into the significance of each feature in predicting the class labels. Additionally, dimensionality reduction was performed using t-sne to visualize the data in two dimensions [69]. t-sne scatter plots were created both before and after balancing to observe the effects of SMOTE on class separation and clustering.

Figure 7.11 summarizes these results. Figure 7.11a shows the class proportions before balancing, highlighting an initial high imbalance. Figure 7.11b depicts the adjusted class proportions after balancing. Figure 7.11c presents the feature importance before balancing. Figure 7.11d illustrates the feature importance post-balancing.

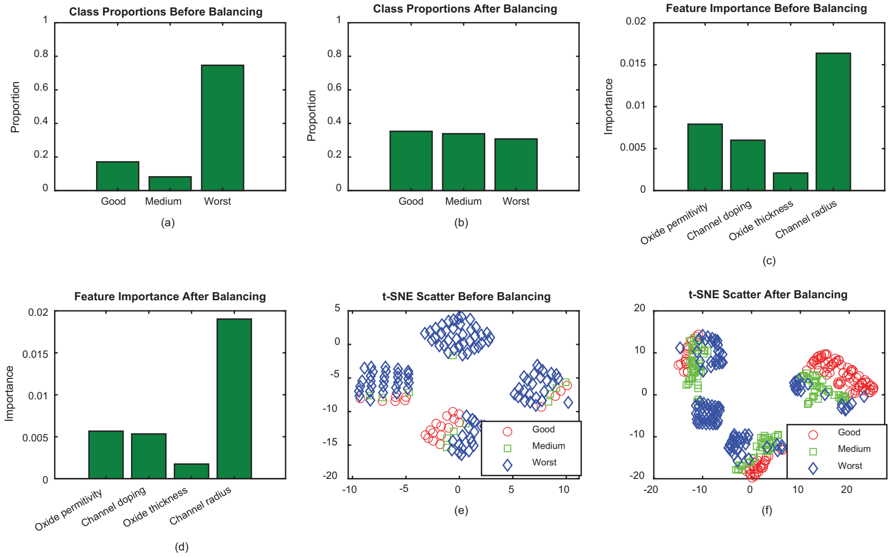

FIGURE 7.11 Analysis of class proportions, feature importance, and t-SNE scatter plots: (a) class proportions before balancing; (b) class proportions after balancing; (c) feature importance before balancing; (d) feature importance after balancing; (e) t-SNE scatter plot before balancing; (f) t-SNE scatter plot after balancing.

Figure 7.11e provides a t-SNE scatter plot of the data before balancing; and Figure 7.11f displays the t-sne scatter plot after balancing. These visualizations and analyses collectively demonstrate the impact of data preparation on the scaling capability analysis of JLMG FETs. As a result, the feature importance analysis reveals that the channel radius exhibits the highest significance, followed by oxide permittivity in the second stage. This indicates that the channel radius plays a crucial role in predicting the class labels of JLMG FETs, while oxide permittivity also significantly contributes to the predictive model. This insight underscores the relative importance of these features in assessing the scaling capability and performance of the devices. Additionally, the data scatter plots reveal a nonlinear distribution of class labels both before and after balancing. This observation suggests that nonlinear modeling techniques may be more appropriate for future machine learning analysis to effectively capture the complexities in the data distributions.

Accordingly, this work utilized a Gated Recurrent Unit with a projected layer (PGRU) to effectively model and analyze the nonlinear patterns and complexities observed in the data [70]. The gated recurrent unit (GRU) was selected for its ability to capture temporal dependencies and handle sequential data effectively, while the projected layer enhances its capacity to model complex, high-dimensional relationships. Hyperparameters were tuned and optimized using a Bayesian optimization approach, ensuring robust performance and efficient convergence [71]. The model was evaluated under various criteria, including Accuracy, $F1$ score, Precision, and Recall, allowing for a comprehensive assessment of its performance and effectiveness in handling the dataset.

In Figure 7.12, the training loss curve (Figure 7.12a) reveals a strong convergence of the PGRU model, with only minor fluctuations and a few spikes, reflecting effective learning and stable performance improvements. The confusion matrix (Figure 7.12b) illustrates that the model performs excellently overall, with only eight

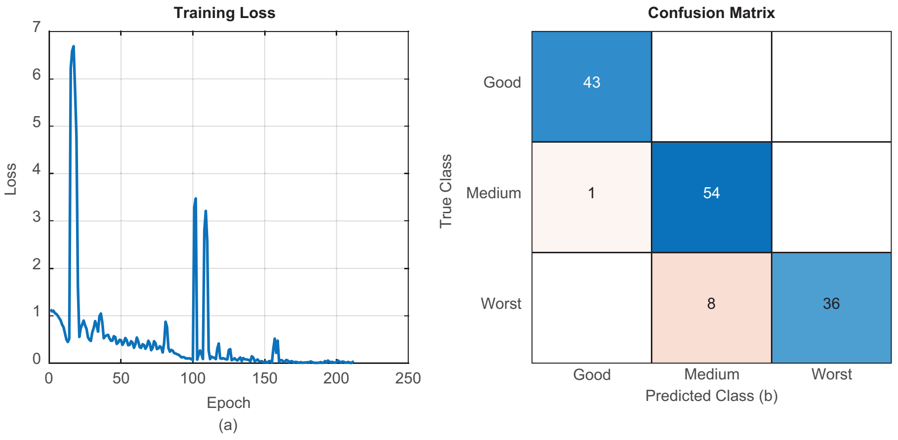

FIGURE 7.12 PGRU model performances: (a) Plot of the training loss over epochs for the PGRU model, showing the model's learning progression. (b) Visualization of the test classification performance, with true vs. predicted class labels.

TABLE 7.1
Performance Metrics for Training and Testing

Metric	Training Value	Testing Value
Accuracy	0.9953	0.9366
Precision	0.9878	1.0000
Recall	1.0000	0.9773
*F*1	0.9939	0.9885
Training time	1.9359 seconds	–

samples misclassified from "Worst" to "Medium" and one sample from "Medium" to "Good." This indicates that, although the model is highly accurate, there is potential for further refinement in distinguishing between "Worst" and "Medium" categories, as well as in improving the classification of "Good" and "Medium" labels.

Table 7.1 presents the performance metrics for both the training and testing phases of the PGRU model. The *F*1 score, used as the objective function during the hyperparameter optimization process, was chosen because it captures the balance between precision and recall, providing a comprehensive measure of the model's classification performance. The training accuracy is exceptionally high at approximately 99.53%, indicating that the model performs very well on the training data. Precision, recall, and *F*1 scores are also impressive, with values of 0.99, 1, and 0.99, respectively. These metrics reflect the model's effectiveness in correctly identifying and classifying instances during training. For testing, the accuracy is slightly lower at around 93.66%, suggesting that the model generalizes well but with a minor decrease in performance compared to training. The test precision, recall, and *F*1 scores are strong as well, at 1, 0.98, and 0.99, respectively, demonstrating that the model maintains high performance on unseen data. The training time is approximately 1.94 seconds reflecting the efficiency of the training and optimization processes. Overall, the metrics indicate that the model is robust and performs effectively across both training and testing datasets.

7.5 CONCLUSION

In this work, we examined the shift from single-gate to MG FETs to enhance device performance and address miniaturization challenges. MG FETs offer improvements in ultralow power consumption, energy efficiency, and low-voltage operation, although they may not yet achieve the drive currents and switching speeds of traditional MOSFETs. JLMG FETs were explored as a more advanced alternative to conventional MG FETs. By eliminating junctions and using a uniformly doped structure, JLMG FETs improve scalability and reduce fabrication costs, offering better electrostatic control. Machine learning techniques were applied alongside 2D numerical simulations to optimize these devices. The obtained *F*1 score of 0.9885 highlights the effectiveness of these models in evaluating transistor performance. This approach provides valuable insights into the scaling potential of JL-DG and GAA MOSFETs, supporting the development of advanced, cost-efficient semiconductor technologies.

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8 Nanosheet Transistors

A New Dimension in Charge Transport

Parul Devi

8.1 NATURE OF WORK: REVIEW

8.1.1 INTRODUCTION

After its introduction in 1959, the FET has mostly been constructed into the silicon plane. The FETs can be organic as well as inorganic. Organic counterparts are similar to inorganic where they are composed of a metal-insulator-semiconductor (MIS) structure. These are often familiar as MOSFET in which the insulator is generally an oxide. The device topologies of both p and n-type OFETs are shown in Figure 8.1a and b, respectively [1,2].

To better control the leakage current, it took the shape of a protruding fin and will now become stacked sheets. In contrast to planar architectures such as FET or MOSFET, the non-coplanar architectures, which are nanosheet and nanowire transistors, can provide an increased device density and increased device performance than the planar transistors. To help downscale the planar devices, finFET was considered as the best technology previously. FinFET establishes better control from gate to channel with reduced gate length and showcases excellent performance at a low value of applied voltage. However, with the current electronic design needs, finFET technology failed to fit within. It posed challenges to the patterning performance, layout, and downscaling costs, which made them undesirable for them to use in circuits. The taller and thinner structure in finFETs posed the greatest hurdle on the path toward better performance and downscaling [1–3]. Figure 8.2 shows the

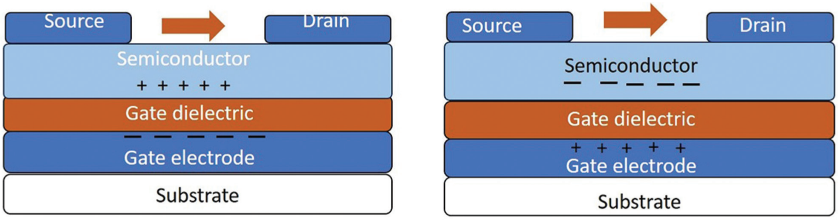

FIGURE 8.1 (a) p-Type and (b) n-type conduction are shown as examples of device topologies of organic field-effect transistors. The red arrow represents the charge flow from source to drain.

DOI: 10.1201/9781003543923-8

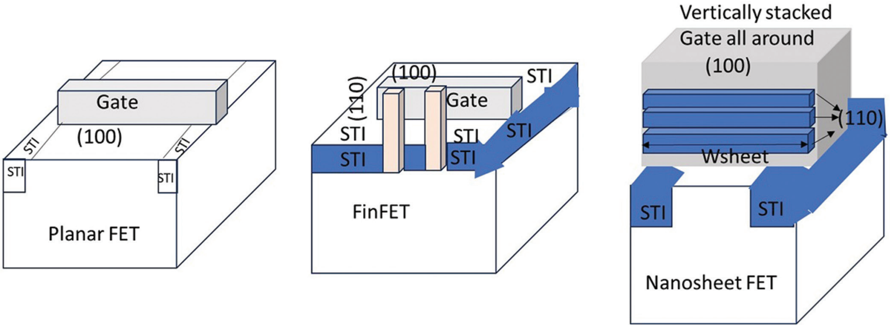

FIGURE 8.2 Schematics of (a) a planar device, (b) a FinFET, and (c) a vertical gate all around the nanosheet field effect transistor.

schematics of a planar device, a finFET, and a vertically stacked bulk gate all around the nanosheet field effect transistor.

To address these challenges with finFETs, gate-all-around (GAA) transistors were developed. Better short-channel control and high current density are attributes of these transistors. The device drive current can be limited by the essential channel breadth of GAA nanowire transistors, which is implicitly microscopic. Stacking several vertical nanowires provides a high drive current, which is required in GAA nanowire transistors. However, the stacking of nanowires is hindered by parasitic capacitance. Soon after designers realized that a new transistor technology i.e. NTs needed to compensate for these limitations. These NTs incorporate a gate assembly that swaddles around the circumference of several nanopillar channels in the areas for better control of channel current go-along. NTs enable fuller depletion in the nanosheet channel regions and reduce short-channel effects [3,4].

NTs have the following advantages.

8.1.1.1 Gate-All-Around (GAA) assembly

NT automation is about the GAA assembly. The conduction strait is surrounded by the excessive k/metal gate of NTs. Over the channel for short channel lengths, the GAA architecture of NTs helps to achieve good gate control. The evolution of NTs from finFET automation-based semiconductor apparatus can be improved in NT construction. Integrated circuit originators welcome the conversion from finFET to nanosheet arrangements because of the advantage of the scaled dimension. The best device architecture i.e. NT is presently accessible in semiconductor automation for outrageous-volume production of integrated devices. With the help of the cadence software, one can design chips based on NT technology [4,5].

8.1.1.2 Variability

The architecture of NT establishes variability in semiconductor devices. To provide variable device width, NT technology is the most suitable one. The device width variation enables design flexibility. A creator has the freedom to carry out a swap between the footstep area, capacitance, and the drive current as per device requirement. How one can vary the capacitance in NTs, the explanation is that it can be managed by employing the breadth of the channel. The decrement in channel width decreases the intersheet parasitic capacitance. Parasitic capacitance reduction is possible in NTs by adjusting the width of the device [4,5].

8.1.1.3 Minimized Dimensions and Excessive Drive Currents

Substantial leveling of logic usual cell with giant drive current capacity provided from the NTs. A higher drive current of NTs provides a specified footstep contrasted to finFET automation. The assembly of nanosheets provides an excessive drive current. An area provides the assembling of a nanosheet-shaped conduction channel, which can only accommodate one fin structure. A larger effective channel width is created by stacking of nanosheets, which increases the device drive current capability in comparison to finFETs [3–5].

1. **Nanosheet Transistors (NTs): The Working Principle:**

   NTs are defined as multi-bridge channel, GAA, or nanobeam transistors. The NTs attained from finFET automation have gainful benefits over finFET and GAA transistors. NTs can shatter the potential solidity boundary of 100 W per square centimeter, which provides the outrageous potential solidity in semiconductor construction for the past decade. NTs push energy as well as power in integrated circuits beyond the limit that is set by finFET technology [5–7].

   There are four steps, which are associated with the fabrication of nanosheet transistors (NTs).

   a. **Epitaxial Growth of Multilayers**:

      In this NT construction procedure, several layers of SiGe and Si are grown epitaxially, which can define the channel of the device. The growth procedure of channels on a lattice is incompatible with the epitaxially expanded materials, which results in NT construction different from the CMOS devices. The sacrificial coating i.e. SiGe detached from the multilayer heaping during the channel release within the metal gate replacement integration step. The entire stacking of multilayers is patterned into a fin structure, which has a high aspect ratio. It was proposed to incorporate shallow trench isolation in NTs to decrease the oxidation-induced fin deformation. Since it increases the speed gain capabilities and drives the current of NTs, is welcomed by many IC designers [6].

   b. **Inner Spacer Integration**:

      An inner space is needed in NT architecture. This inner space is made of dielectric material, which can isolate the gate from the drain and the source. The integration process of inner space recesses the outer portions of the SiGe layer, which can create small cavities. These cavities are filled with the dielectric materials later [6].

   c. **Nanosheet Channel Release**:

      In the NTs fabrication process, these nanosheets are separated for the release of the channel by etching away the SiGe part of the multilayer [6].

   d. **Metal Gate Integration Replacement**:

      The last step i.e. metal gate integration replacement is significant to increase the speed gain of the NTs at constant power. A work metal is deposited and patterned around and in between the layers of nanosheets. The work function selection of metal influences the vertical height of the nanosheet stack [6].

2. **Issues and Recent Progress in NTs**:

   No doubt about the great success of finFET, finFET was invented more than a decade earlier. The first commercial introduction was in 2011 at the 22 nm node by Intel and later by Samsung, TSMC, and others. Since then, it has been the go-getter of cutting-edge silicon logic in these final stages of Moore`s scaling law [5,6].

   a. **Shortcoming of finFETs**:

      As excellent as finFETs are, they have their problems.

      i. Design limitation as it was not an issue for the old ‘planar’ transistor. To figure out this complication, we have to comprehend that there be on every occasion a back-and-forth surrounded by energy consumption, complexity of production, cost, and transistor speed. This back-and-forth is obliged to be done along the channel breadth, which is termed W_{eff} in device circles design. Large breadth provides to operate additional current and faster switching of the transistor now and then/again. But it as well requisite a more difficult and extravagant assembly procedure.

         In a consistent circuit, we can assemble this back-and-forth by directly adapting the channel geometry. But finFETs flexibility is not as much as it is required. The metal links these link transistors to configure devices to build them in stratification beyond the transistors themselves. As a consequence, finFETs can`t extend exceedingly in height i.e. equivalent to width in planar designs without interfering with the interconnect layers. Nowadays chip creators acquire rid of this drawback by producing discrete transistors that have innumerable fins.

      ii. Other shortcoming of finFETs is that the aforementioned gate encompassing the quadrilateral silicon fin on three edges, which departs the undersurface attached to the frame of silicon. It makes a few leakages of current pass during the transistor is switched off. Numerous FET investigators claimed that the gate needed to surround it, to gain eventual domination above the channel area.

         Around 1990, researchers took this idea to a logical conclusion. In the same year, the first silicon device with a gate was reported by investigators, which is near the channel area. Since that time, a lot of investigators have contributed to so-called GAA circuits. The time 2003 onwards, investigators tried to shrink leakage by turning the channel area into a small nanowire that spans the source and drain, and it can be encompassed by the gate on all edges.

Little opportunity can be provided by a nanowire for electrons to get away while possessing the transistor turned off when it should be switched off. At the same time, it also provides little room for electrons to flow by keeping the transistor on, limiting current, and slowing switching [7–9].

We can obtain additional W_{eff} and so the current, by layering nanowires over and above each other. In 2004, Samsung engineers unveiled the configuration of this version, which is called multi-bridge channel FET. But it also had several limitations such as fin-FET's fin, the stack cannot get much high or it can interfere with the interconnect layer [8–10].

In 2006, a better idea was demonstrated by the engineers. A stack of thin films was used by utilizing a large number of nanowires to overpass the source and drain. It was pre-owned to increase the channel width in a compact transistor while sustaining compact command of the leakage current and therefore produces a superior-implementing, less energy circuit. For different, each addition of a nanowire increases the capacitance of the circuit by reducing the shifting pace of the transistor. As a consequence of the complication of manufacturing nanowires very limited, they can frequently fetch up being rough around the edges. This surface roughness can impede the charge carrier speed [9,10].

Nanosheet design provides another beyond advantage by restoring the flexibility lost in the transition to finFETs. To amplify current or slight to restraint capacity utilization, sheets can be fabricated wide. It was constructed in stacks of three in the size range from 8 to 50 nm across [9,10].

8.2 METHODOLOGY

It has been acknowledged for plenty of years that confinement in small structures requires quantum mechanics, which leads to quantum transport. Over extravagant centuries, it has remained that the FET does not need to be described by quantum transport. In the long ago several decades, contemporary varieties have tended to be superintended by quantum confinement and the proceeding restrictions to the usual classical explanations. Adding to that correlation and confinement leads to a need to describe the transport by quantum method as well [4].

Many discussions have been regarding the part of quantum effects and quantum transport in FETs. Nevertheless, how immense is the quantum hole (or electron) boiled down to the problem? Classically, the electron size has been contemplated with time but has been established at ~10^{-18} m. So, this theory will be unreasonable for quantum particles, and the electron size depends on the quantum mechanical representation of the wave packet. A great consideration about the size is in the range of 3–7 nm [4]. The quantum transport in NSFETs has been explained in the flow diagram as shown in Figure 8.3.

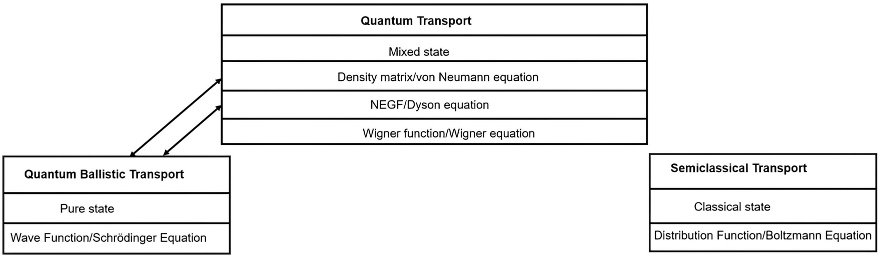
Quantum Transport
Mixed state
Density matrix/von Neumann equation
NEGF/Dyson equation
Wigner function/Wigner equation
Quantum Ballistic Transport
Pure state
Wave Function/Schrödinger Equation
Semiclassical Transport
Classical state
Distribution Function/Boltzmann Equation

FIGURE 8.3 Flow diagram to explain the quantum transport in NSFETs.

According to Moore's law, the concept of a 5 nm node is discussed for microelectronic devices. It becomes a problem for the MOSFET, where ~5 nm electron can be embedded into the classical magnitude of reversal coating that is ~1 nm potential well. To solve this problem, Poisson's and Schrödinger's equations require a self-consistent solution. To pursue this, the self-correspondent perspective introduced for electrons in an n-channel part of the Si MOSFET splits the six same energy levels valleys of the conduction band. The hefty mass handling of two valleys is usual at the interface of the oxide-semiconductor from a single set of lowest energy quantum levels among the four valleys with the slight mass usual to the boundary. All MOSFETs will show this quantization from such calculations. In everyday operations, quantization is not observed for several reasons. The quantization is a second-order effect as the transport direction. This calculation is a one-electron effect, which is appropriate for having no inversion density [10,11].

Another quantum effect i.e. many-body interaction arises in the presence of inversion density. The energy levels are lowered by the self-energy of the carriers, while quantum confinement raises these levels. These considerations estimate this quite complicated. In today's devices, a common situation arises because of making the most of tensile strain to expand the dissociation between four-fold (higher energy) and two-fold valleys (lower energy). Numerous modern simulation collections through clever manipulation describe the scale of the electron but not without deviation. The hole and electron energy inhabitants are an aggregation of the solidity, which is encumbered by the potential at every notability. The productive potential that disentangles the presentations of these circuits, can move the appearance of the electron wave packet from the electron to the potential. Effective potential becomes apparent from the electron's size that appears in those packages. These deliberations make it perceptible that confinement ramifications embellish corresponding to the hole or electron wave packet. The quantum effect plays a considerable role in today's ultrasmall devices. Further examples become visible in FinFETs, which are well received at this moment. The channel is turned from FinFET on its slanting, which makes the inversion coating amplify up either the edge of the fin or smooth over the peak. The turnoff becomes more effective when the two potentials are working together along the gate potential on the other side of the fin. If there are two inversion layers in a normal state, it can alter into a single inversion layer in the bulk of the fin. The central inversion layer is the preferred state for sufficiently thin fin and medium density. The basic nature of FET changes from a surface-oriented device to a bulk-oriented device because of the quantum effects. It added the benefits of less scattering from the rough interfaces. A true quantum effect i.e. tunneling has been around for some time. Tunneling through the gate oxide is a concern in the past. The barrier between the FET channel and gate metal is no longer a simple rectangular barrier but it becomes triangular or trapezoidal in the presence of high electric fields across the gate oxide. As long as we have had MOSFETs, this tunneling has been known to be a problem in thin dielectrics. Continuous downsize of the device becomes more interesting, which is direct tunneling between source and drain. The resonant tunneling between the drain and source was observed caused by the localized condition, which is the tendency of microscale circuits and creates undeviating tunneling connecting the source and drain. High κ dielectric adoption was an uninterrupted retaliation to the complication of gate tunneling in gaunt oxides, which is essential in the scaled devices. As we endure progress accompanied by Moore's law, the quantum effects appear in greater quantity. Nevertheless, it is ambiguous how the difficulty of source-drain tunneling will be communicated. As quantum mechanics is notably an outlander hypothesis, it can be treated in isolation, however, it is not at all evident. So we can expect that many quantum effects interact with each other as well as with the understanding of how the FET operates [11,12].

8.2.1 ELECTRONIC STRUCTURE AND ELECTRONIC TRANSPORT

The concept of multiple gates brought forward an open field that can be done with quantum wires and GAA automation. The initial quantum wire device was a gaunt channel MOSFET of 10 nm breadth. The gate length of silicon on the insulator is 250 nm and the Si coating is 7 nm, which announced the device's purpose to study quantum effect in ultra-small MOSFET. There was no typical dopant in the channel as the strait doping was as little as 1015 cm^{-3}. Although, the studied channel width range is from 1.25 to 43.75 nm. Reduction in channel width below ~10 nm increases threshold voltage. Around 2004, both theoretically and experimentally, the GAA Si nanowires appeared to become visible. The height and width of manufactured wires were around 12 and 20 nm and the insignificant gate length was around 100 nm. These were encompassed with oxide and the gate was beside a trigate in contrast to GAA. An outstanding subthreshold slope was shown in comparison to a planar device. Even with the variation in diameter wires, these circuits had similar bulk-to-surface channel results. These nanowires show no increase in mobility with the simulations. Moore's Law outcomes from a profitable law instead of an automation law. As the technology proceeds, to minimize the price of Si, the gate periphery should be greater than the Si region, which make a long story short the price of Si itself to proceed Moore's law. It contributes the adaptation to FinFETs, which has revealed that the economic requirement cannot be satisfied from the nanowire laid on the surface of Si. That is because a single layer of circular wires is heavy ample to overcome the height advantage of FinFET. It can be resolved by having vertical wires, which is a more demanding constructing automation. A more acceptable process is the stacked nanowires. The stacked nanowires were good, but not much preferred as FinFET. It changes accompanied by the nanosheet FET, that is a large number of squeezed wires for which the upright thickness was considerably underneath than the breadth of every wire. However, the expression nano-sheets came behind from the joint attempt of Samsung, Global Foundries, and IBM. A different collection of strain probabilities arises in the aforementioned stacked GAA apparatuses by utilizing other materials such as Ge and SiGe. Generally, the substrate stack undergoes punch-through by the drain-source bias that results in leakage, for which the design of penetrate-through stopping coating is pre-owned. The bottom oxide layer was accustomed to anticipate this action and superior domination. A stack nanosheet that has four nanosheets is shown in Figure 8.2 [4]. The preferred and usual is to use three nanosheets. The oxide created to use better threshold slope and less drain-induced barrier lowering. This led to the announcement of IBM's 2 nm node technology using their nanosheet and oxide spacer layers. This approach results in a nanosheet of 40 nm wide and 5 nm thick accompanied by a successful gate stretch of 12 nm. As anticipated, this automation will become visible in mainline manufacture in 2024. Further automations, which are formulated by various epitaxial and deposition methods are being examined for the nanosheets. A little while back, the monolayer 2D transition metal dichalcogenide (TMDC) materials were considered in this confederation. These 2D substances such as WS_2 and MoS_2 provide the eventual in nanosheets because the coating thickness in these 2D materials is less than a nm. These materials have reasonable mobilities, velocities, and a sizeable band gap [4]. It is possible, as crucial as the obstacle is to retain the p-channel and n-channel transistors of CMOS pair compact closely. One of the suggestions has created to various proceeds towards, possibly leading to the layering of p and n circuits in addition to each other to a certain extent of the nanosheet layer. Forksheet technology is one of the approaches to it that utilizes a self-aligned common gate between two devices.

8.2.2 THE DRIFT-DIFFUSION (DD) MODEL

In this segment, we will discuss the DD representation for organic semiconductor NTs. The presentation of consecutive sensing is accompanied by dissemination indications in which the resolution creator gathers display up till it affects one or the

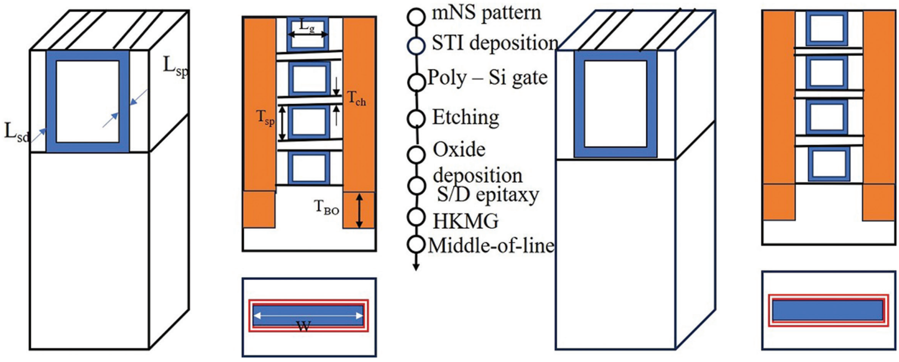

FIGURE 8.4 3D scheme and cross-section of the multi-nanosheet FET (a) bottom oxide transistor and (b) no bottom oxide transistor.

other lower or higher stopping boundaries, and afterward, it concludes and selects the alternatives that correspond to the boundaries, known as the drift-diffusion model. In perceptual and utilization assignments, the process of drift is connected to the choice that is objectively correct and accumulates correlated to the comparable retrial of the options respectively. This model accepts that the concluding confines are persistent past the usual finishing time. Nonconstant confines have been used in many papers that better fit the data. This model works for different devices such as organic and inorganic for different applications. To solve a set of equations, the DD model is enclosed by the defined element technique utilizing the trading software TiberCad. Furthermore, the DD representation can investigate charge carrier mobility imbalance in organic solar cells. Along with that, the circuit-level modeling for recognizing the short conductivity areas in organic wafer-thin films results from electric carrier confining. Inside the chapter, we initiate by generating a construction for a generated, which is a corresponding mesh composed of numerous components, for which DD mathematical problems are pertained and need to be resolved. Here, we have a tendency to consider a 2-dimensional (2D) bottom-gate-bottom contact construction. This 2D device is shown in Figure 8.1 and mesh representation is shown in Figure 8.3 [2].

The Poisson and continuity equations are the main equations for the drift-diffusion model, which can be written as

$$\nabla.(\varepsilon\nabla\varphi) = (p - n + N_D - N_A + p_t - n_t) = \rho \tag{8.1}$$

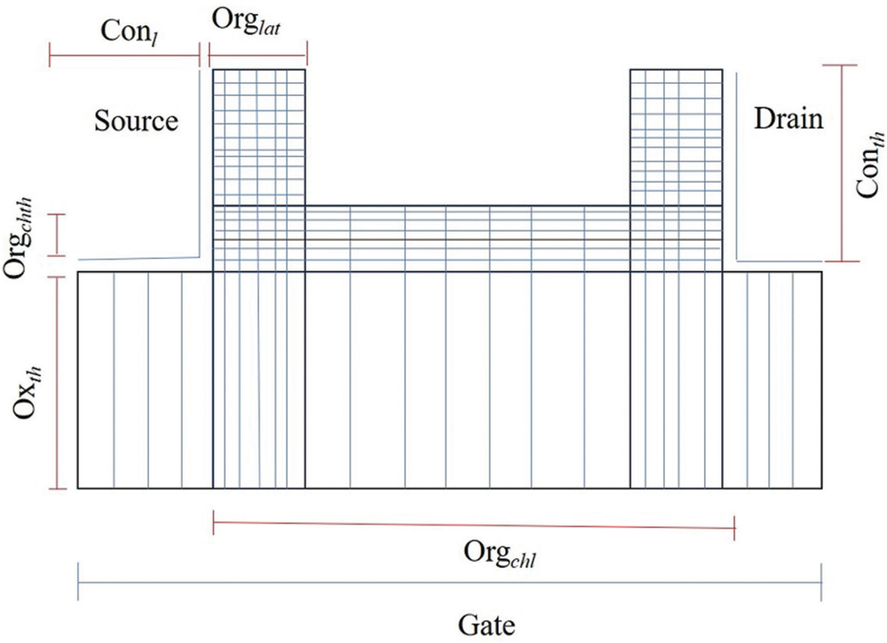

FIGURE 8.5 Bottom gate-bottom contact (BG-BC) meshed representation.

$$\nabla . J_n = \nabla . \left(\mu_n n \nabla \varphi_n\right) = -R + G \tag{8.2}$$

$$\nabla . j_p = \nabla . \left(\mu_p \mathrm{p} \nabla \varphi_p\right) = R - G \tag{8.3}$$

In these equations, ε is the permittivity, φ is electronic potential, e defines electronic charge, and p and n define the hole and electron mobile charge densities. The donor and acceptor concentrations are defined by N_D and N_A, respectively. p_t and n_t represent the term density and define charge density. In Equations (8.2) and (8.3), μ_p and μ_n are charge mobilities for hole and electron. R and G are the recombination and generation terms.

For our transistor analysis, recombination and generation terms will not be considered. Unipolar devices are the focus of this work. On sweeping the barrier electromotive force, we start regarded by a scrape on the drain voltage at every gate. In this process, the DD equations are solved self-consistently and the drain voltage will be calculated [2].

8.2.3 GAUSSIAN DENSITY OF STATES (GDOS)

Into and out of an arbitrary dispensation of constrained positions, charge transport in NTs relies on a hopping mechanism. The DOS can be described by a Gaussian function, to have an appropriate description of charged ions, which can be expressed as

$$g(E) = \frac{N_0}{\sigma\sqrt{2\pi}} \exp\left(-\frac{E^2}{2\sigma^2}\right) \tag{8.4}$$

Here, N_0 defines location solidity, E is the energy, and σ is the energetic disorganization individually. The range of energetic disarrays in the case of organic semiconductors varies in the middle of 30 and 100 meV. It depends on the anatomy of the substance. This is because polymers can tolerate higher levels of disorder compared to small molecules. As we move from small to large disorder, it causes an expansion in the irregular dispensation of positions that move more distant elsewhere from these captivate levels. Because of that, a few of the places might behave as confined positions, which affects comprehensive charge transport. Furthermore, charge mobilities depend on the carrier density, thermal factor, and applied field. The mobility obsession on the carrier density and thermal factor is affected by the DOS. Therefore, it is important to have a correct description of the appropriate amount of disorder and DOS depending on the material chosen [2–4].

8.2.4 THE TRAP MODEL

Among the major representatives that can influence the device's production is the charge carrier trapping in organic semiconductors. They can have different effects on the performance of the device such as causing hysteresis, degrading mobilities, and leading to threshold voltage shifts, which depend on the energy associated with trap states. Stability over a large period is also one of the major issues in organic semiconductors. Especially, one that incorporates n-type material as the active region. Because of this compatible argumentation established on these organics has been shown demanding to attain. To incorporate confines in DD simulation and their results, which can be identified from the transfer attributes of OFET is imperative. Our DD simulations, which have traps are designed as follows:

i. When an electron is trapped, a neutral trap becomes negatively charged.

$$n_t = \frac{N_t}{1 + e^{\frac{(E_c - E_{\mathrm{ln}}) - (E_{F,n})}{K_b t}}} \tag{8.5}$$

ii. In contrast to that, when a hole is trapped, a neutral trap becomes positively charged.

$$p_t = \frac{N_t}{1 + e^{\left[-\left(\frac{E_v + E_{\mathrm{lp}}) - E_{F,p}}{K_b t}\right)\right]}} \tag{8.6}$$

iii. The density is simply defined for fixed charges. It can be either positive or negative.

N_t defined the density of traps, and E_{tp} and E_{tn} are hole and electron trap energy levels. $E_{F,p}$, and $E_{F,n}$ are the quasi-Fermi energies, K_b is the Boltzmann constant, and T is the temperature. The confine levels can be defined by the credentials to the valence or conduction bands (E_v or E_c).

For the investigation of inorganic materials and devices, these models have been used. To justify their use for the investigation of transport of charges in organics, it should be able to appear the corporal explanation of certain phenomena that arise in the organic materials and devices. One such event is the presence of interface dipoles, which survive as a consequence of inhomogeneous dissemination of charges at an exterior. These dipoles can happen at organic-metal interfaces, organic-organic, and dielectric boundaries.

$$\Delta_d = \frac{q m_d \cos\theta}{A_d \varepsilon} \tag{8.7}$$

In Equation (8.7), q defines the electronic charge, m_d defines the electric dipole moment (which can be defined in Debye units and depends on the interspace in the middle of positive and negative charges), the angle of the dipole for the surface is defined by θ, A_d the area of exterior charge, and finally, the dielectric constant of dipole layer is defined by ε. An exterior region of charges presents at a boundary and uninterrupted Coulomb attraction, opposite sign charges are located on the obverse side. Hence, it can be defined as

$$\Delta_d = \frac{q}{A_d \varepsilon} \tag{8.8}$$

Both Equations (8.7) and (8.8) are almost identical except for the angle θ, which allows us the representation of fixed charges i.e. the effect of dipoles in our simulations. Separation between charges is within a fraction if the assumption is valid. Here, we show that the threshold voltage is affected by fixed charges and so the field-effect mobility, which allows us to account for interface dipole effects [11,12].

In our DD simulations, regarding the modeling of trap states within organic materials a similar connection can be achieved. These defects can be energetic, structural, or a combination of both. To account for the redox states, these trap models can also be used. Organic materials can go through redox reactions. The transfer of electrons from (i.e. oxidation) or to (i.e. reduction) involved in the reactions by the host material. The investigation of organic electrochemical transistors (OECTs) relies on transitioning between redox states that have been done for biological applications. The intermediate energy levels, which are associated with the energy levels of organic materials in redox states formed inside the band gap. When the device is operated under an external potential, intermediate levels act as doping or de-doping centers. To account for the charge carrier trapping and de-trapping, our DD trap models can be used to account for these effects as well [2, 13,14].

Equations (8.5) and (8.6) stand, if the simulated traps are intended to represent these defects. To represent the redox reactions, both E_{tn} and E_{tp} in Equations (8.5) and (8.6) are replaced with E_{redox}. Furthermore, molecules are represented by N_t, which means that N_t has to be equal to N_0 from Equation (8.4). N_t can be somehow lower or higher. A classical description of the density is represented by Equations (8.5) and (8.6). The density description in organics is of a quantum mechanical nature, which is linked to the delocalization of wavefunction, in which molecules are charged by a fractional charge. This results in the density value N_t higher or lower than the molecular density level N_0 [2,13,14].

8.2.5 THE MOBILITY MODEL

DD simulation describes how the charges can proceed enclosed by a transistor strait. To choose from TiberCad, multiple models are available. There are two models available specifically for organic semiconductors for such investigations. An overview will be presented for both representations and how the determination can be taken possession to utilize affecting ahead accompanied by simulations [15].

8.2.5.1 The Pasveer Mobility

Pasveer developed this representation. This model is acquired as a parametric pertinent of numerical emulsions for a method of mastering mathematical problems executing the Miller-Abraham leaping models in the middle of confined conditions with a Gaussian energy dispensation.

In this representation, the mobility depends on the following equation:

$$\mu\left(T,\,\rho,\,f\right)=\mu\left(T,\,\rho\right)f\left(T,f\right) \tag{8.9}$$

$$F>\frac{2\sigma}{ea} \tag{8.10}$$

8.2.5.2 The Poole–Frenkel Mobility

$$\mu = \mu_0 e^{\left(-\frac{\Delta - \gamma\sqrt{F}}{kT}\right)} \tag{8.11}$$

8.2.6 Simulation-Related Remarks

Here, we will place out a few simulations-connected comments. A BG-BC transistor architecture will be contemplated here. The device can be split into two regions (a) organic and (b) the oxide. The organic area can be additionally broken into two, in which the peak segment is huge and the lowest segment is accustomed to design connection results. Regarding this, they all are considered as the device's boundaries (i.e., physical lines). We do not take into account the bulk representation of the contacts as there is no change in expressions of current-voltage features. This exclusion will allow us to obtain improvement in simulation times.

2D meshed delineation is pertaining to the subsequent implement aspect designations: thickness of the oxide ($\mathrm{Ox_{th}}$), length of the channel ($\mathrm{Org_{ch\_l}}$), organic near contacts lateral dimension ($\mathrm{Org_{lat}}$), thickness of the contact ($\mathrm{Con_{th}}$) and length of the contact (Con_l). All the dimensions are pre-defined and always fixed except $\mathrm{Org_{ch\_l}}$ and $\mathrm{Ox_{th,}}$ which are changed regarding experimental values [15].

8.3 IMPACT OF DIFFERENT PARAMETERS

The most complex system in the world is the central processors lodged accompanied by millions of transistors. The transistor density along with the performance must be enhanced to fulfill the speedy-swaping purchaser requests for microscopic and outrageous-accomplishment instruments. A 7 nm automation node was developed to attain FinFET automation. Future bottom automation nodes for instance 5 or 3 nm will look towards a few expressing oppositions such as patterning, cost, layout, self-heating effects, transistor performance, and severe short-channel effects. Another limitation with FinFET is that the gate balances three sides of the rectangular Fin because the surface side of the Fin moves closer in proximity accompanied by the substrate. The computing world tries to align with the advancement of transistors for better performance. In works of literature, a lot of studies have been done on the electrical performance of transistors with the variation of different parameters. This section describes the impact of different parameters on the charge transport and electrical characteristics of NSFETs [12,13].

8.3.1 Nanosheet Width/Thickness Scaling and Substrate Materials

IBM research group first introduced the concept of NSFET in 2015. This was empirically revealed as the earliest at any point horizontally layered GAA NSFET. It is contemplated as a significant competitor to restore the FinFET automation at the 5-nm node and further on. GAA NSFET has the major advantage of a large ratio of W_{eff} (virtual strait breadth)/LFP (layout footprint). The first GAA NSFET had a barrier stretch of 12 nm and approached polypitch (CPP) of 44/48 nm. The quantum mechanical effect comes into the picture as the technology goes beyond 7 nm [16,17]. The depletion in strait breadth decreases the ballistic current in NSFET, which can be determined as

$$I_{\text{ballistic}} = q \cdot N_{\text{inv}} \upsilon_{\text{inj}} \tag{8.12}$$

Here, q – electron charge, N_{inv} – inversion charge density, υ_{inj} – inection velocity.

The injection velocity in p-type SiGe NSFETs is inversely proportional to the nanosheet width. However, n-type Si NSFETs do not depend on the nanosheet width. Injection velocity can also be enhanced in NSFETs from the strain in the channel. Ge-based p and n-channel GAA NSFETs have higher charge mobility than the Si and SiGe materials. The horizontal Ge-GAA NSFETs was fabricated by low-pressure chemical vapor deposition (LPCVD). GeSn has higher mobility than Ge, which has emerged as a p-type channel material for vertically stacked GAA NSFETs. The improvement in hole mobility of GeSn was observed because of the introduction of Sn into Ge, which helps to reduce the effective mass of the hole. NSFETs exhibit low RC delay and higher I_{ON} (ON current) at 7-nm technology nodes in comparison to the FinFETs. Intrinsic delay i.e. RC can be computed as:

$$\text{RC} = C_{\text{gg}} \cdot V_{\text{dd}} / I_{\text{ON}} \tag{8.13}$$

Here, C_{gg} defines gate capacitance and V_{dd} represents the operating voltage. It indicates that at the sub-7 nm technology node, NSFETs outperform FinFETs. These NSFETs exhibit outstanding potential to scale down the performance improvement in comparison with FinFETs for future applications in analog/digital integrated circuits [18,19]. The fabrication process of vertically stacked GAA NSFETs is different from FinFETs because of the process of channel release by selective sacrificial layer etching. The selective sacrificial layer is inserted between nanosheets in vertically stacked GAA NSFETs. Two different techniques are commonly used for the etching processes such as vapor HCl and chemical dry etching. These techniques do the unintentional etching of nanosheet channels, which varies the nanosheet channel thickness. Vertically stacked NSFETs within a single substrate create an issue of different nanosheet widths. High electron density, low threshold voltage, and higher I_{ON} in Si-NS-FET can be achieved in a low nanosheet width of 3-nm stacked nanosheets. Due to poor gate controllability, a higher nanosheet width results in an increase in threshold voltage. Gate-source parasitic capacitance (C_{gs}) was found to be increased by scaling down the nanosheet width. Interface trap density (D_{it}) is also affected by nanosheet width in staked lateral NSFETs, which is due to the induction of diffusion of Ge into Si-nanosheets from the thermal process, which is carried out before the channel releasing process. Narrow-channel NSFETs have lower D_{it} than that wide-channel devices. An increment in the nanosheet width of stacked lateral NSFETs decreases its gate control over the nanosheets. The impact of nanosheet width is more on short gate length devices [16–20].

Recent literature also investigated the impact of channel crystal orientation in addition to the channel width on electrical characteristics of vertically stacked horizontal p-type Si and Ge NSFETs. Higher I_{ON} is observed in vertically stacked horizontal NSFETs in comparison to the single NSFET for both Si and Ge channels. Si and Ge channel crystal orientation also plays a part in determining the I_{ON} of the devices. [111] crystal-oriented Si-channel exhibits higher I_{ON} than [100] and [110] in vertically stacked horizontal p-type Si-NS-FET. However, Ge-NS-FET [100] provides the highest I_{ON} than [110] and [111]. Channel width increment results in the decrement of I_{ON} for both Si and Ge-channel NSFETs. Due to poor gate control of nanosheets, the channel width increases the source-to-drain tunneling rate, which increases I_{OFF} in both p-type Si and Ge channel-based NSFETs.

The electrical characteristics of NSFETs can be significantly changed by the presence of different wafer materials because of the different carrier mobility of the substrate material in the channel. The elimination of dopant intrusion from the wafer results in higher electron mobility of NSFET with silicon on insulator (SOI) wafer in the nanosheet channel. Diffusion of dopants into the channel from the wafer during annealing treatment provides the lowest electron mobility in NSFETs with PTS-Si (Punch-through stopper-Si) substrate. The enhancement of the coulomb scattering effect as a result of the diffusion of dopants from the PTS-Si substrate to the Si-nanosheet channel degrades the electron mobility in the nanosheet. Therefore, higher transconductance and drain current were observed in NSFETs with SOI and SSR-Si (Super steep retrograde-Si) compared to the NSFETs with PTS-Si substrate. For the smaller width of nanosheet in vertically stacked GAA NSFETs with SOI and PTS-Si substrates, the off-current I_{OFF} will be minimal in these devices compared with SSR-Si substrate-based NSFETs due to the absence of parasitic channel. The lowering of energy barrier in the parasitic channel for NSFETs with SOI wafer exhibits higher drain conductance (g_{ds}) for wider width of NSFETs [20,21, and references therein].

8.3.2 Parasitic Nanosheet Channel Height and Gate Length Scaling

Parasitic nanosheet strait is accommodated underneath the upright layered nanosheet straits in NSFETs. The parasitic nanosheet channel strait (H_{ch}) notably influences the DC features of the upright layered GAA NSFETs. The effect of H_{ch} on DC accomplishment of upright layered GAA NSFETs was noticed in literature and it was found that I_{ON}/I_{OFF} ratio enhanced accompanied by expansion in H_{ch}. Base-level doping is used to reduce the result of parasitic nanosheet channels in upright-layered GAA NSFETs. In addition to that punch through can be minimized, which increases the doorstep voltage of the exploitative nanosheet strait. An increment in H_{ch} increases the RC delay and gate capacitance of vertically stacked GAA NSFETs. I_{ON}/I_{OFF} ratio can be enhanced with large H_{ch} and high ground plane doping [22,23].

Reliability and performance with aggressive gate length scaling are one of the most serious concerns in GAA NSFETs because of the self-heating effect. Among all FETs, GAA NSFETs exhibits the highest electron velocity as a result of the magnificent sub-band occupation and improved handle of the gate over the nanosheet strait. Among different FETs, GAA NSFETs exhibit better I_{ON}/I_{OFF} ratios for similar instrument attribute dimensions. Argumentative length smaller in size in NSFETs results in the contraction of threshold voltage, which escalates the I_{OFF} and as a consequence deteriorates the I_{ON}/I_{OFF} ratio. Due to the large nanosheet width per layout footprint and reduced parasitic capacitances, GAA NSFETs offer a high drive current compared to all FETs. The capacity inversion under ON situation surroundings outcome in the enhancement of I_{ON}, which is due to large effective nanosheet width. Literature also indicates the influence of tri-gate, omega- gate and GAA constructions on the expandability of NSFETs. The outstanding scalability is also observed in NSFETs with tri-gate and omega-gate structures in comparison to the other FETs [23–26].

8.3.3 TEMPERATURE, METAL GATE WORK FUNCTION, AND DEPTH OF SOURCE/DRAIN METAL

AC and DC accomplishment of NSFETs can be significantly affected by the temperature. The I_{ON}/I_{OFF} ratio of n-type $Si_{0.15}Ge_{0.85}$ NSFET increased from 5×10^7 to 5×10^8 at $V_{DS} = 0.5\,V$ when the temperature is varied from 300 to 80 K. An increment in temperature results in an enlargement of I_{OFF}, which degrades the performance of the circuit. Impurity scattering and phonon scattering are two predominant parameters in n-type $Si_{0.15}Ge_{0.85}$ NSFETs. Impurity and phonon scattering dominate at two different temperatures 300 and 80 K respectively. Enhancement of phonon scattering degrades the carrier mobility and lattice parameters of the device. The nanosheet's thermal conductivity decreases with an expansion in temperature. The nanosheet width increment assists in diminishing the device's thermic resistance and improvement of $I_{ON.}$ The consequences of temperature on DC production of upright GAA NSFETs exhibit the least threshold voltage in comparison with NSFETs with omega-gate and tri-gate structures. To improve the scalability towards the 3-nm technology node, the vertically stacked NSFET with GAA technology is the most promising one [27,28].

The threshold voltage can be modulated with the two important parameters: metal gate work function and metal gate thickness. The increment in the work function increases the threshold voltage in n-type upright assembled GAA NSFETs while the increment in the gate metal work function decreases the threshold voltage of p-type vertically stacked GAA NSFETs. The gate metal work function increases the gateway voltage of the circuit, which diminishes the on and off current of the circuit. The ratio of bottom side nanosheet breadth (W_{bot}) and top side nanosheet breadth (W_{top}) further regulates the gateway voltage and existent drive current together of p and n channel upright GAA NSFETs. All p and n-channel NSFETs accompanied by substantial W_{top} and W_{bot} exhibit low threshold voltage compared to smaller W_{top} and W_{bot} NSFETs. As a consequence of the sizeable essential breadth of the channel, both p and n channel vertically stacked GAA NSFETs decrease whether the shift of the metal gate work function from the doorstep voltage. Since the carrier density changes considerably with the dissimilarity in metal gate work function, which is the considerable cause for the shift of drive current and gateway voltage in NSFETs. Both p-type and n-type NSFETs display a counteractive trend in electron density [26–28].

The source-drain parasitic resistance (R_{SD}) can be drastically increased with the smaller size of the nanosheet/channel breadth or the shrink of the fin accompanied by the cell height reduction, which can degrade the DC performance of multi-gate transistors as well as NSFETs. Beyond the 7-nm technology node, source/drain (S/D) metallic structure can be used to minimize effectively. The metal depth (T_{M0}) (S/D) can significantly affect the AC/DC performance of NSFETs. The drain current of both p and n channels in GAA vertically stacked NSFETs can be increased with the T_{M0} increasing from 0 to 50 nm. This might be due to increased gate capacitance as a consequence of the increment in T_{M0}. The increment in T_{M0} also minimizes the R_{SD} and RC delay of the vertically stacked GAA NSFETs. High T_{M0} and low contact resistivity are crucial for strengthening the I_{ON} of upright alignment GAA NSFETs [28–30].

8.4 CHARGE TRANSPORT IN NANOSHEET TRANSISTORS

Despite that, the carriage charges in NTs are of importance for several prospective implementations in electronic circuits. The foundational procedure of the charge conveyed through different layers, which are commonly distinguished by a composite nanostructure is still receptive. A little while back, it came across that a little bit of nonconductive scraps can also hold up conductivity by presuming tunneling routes. The nanoscale morphology of NTs is not only multiplex in addition to the interlinkage connecting charges traveling across different layers and molecular assembly and the Coulomb interlinkage linking charges themselves. A workable path to investigate the construction-accomplishment relationship has been via electrostatically gated thin-film field effect transistors, which permit the investigation of freight charges techniques as a purpose of charge carrier density and morphology. Despite the indirect nature of such measurements, it advances our empathy of freight charges through NTs remarkably. The charge transport nature in nanosheet transistors depends on a handful of predominant characteristics like the charge mobility model and the description of the density of states. Therefore, specific models that can describe the electronic possessions of nanosheet transistors must be examined. In this chapter, we have pre-owned a drift-diffusion model for the electrical delineation of NTs utilizing stacked nanosheets [30–34].

8.5 CONCLUSION

This chapter confers the execution of NSFETs and accompanies it with further nano-structure transistors such as FinFET and NWFET. Among all of them, the NSFET is the nano-dimensional transistor that is more acceptable for the recently developed 3 nm node automation than the FinFET and NWFET since better electrical parameters such as DIBL, subthreshold swing SS, and threshold voltage (V_T) due to this node of automation. NSFET also has additional dielectric in the constructions and hence is more competently current. In addition to that innumerable-threshold voltages can be utilized in NSFETs under the variety of metals in numerous gates. To intensify the production of NSFETs, at rock bottom, the dimensions, source, and drain ought to contain metals [34–36].

Different parameters such as the impact of substrate materials, the effect of geometrical scaling, parasitic channel height, and the impact of thermal and source/drain (S/D) metal depth consequences on analog/digital accomplishment of

NSFETs were also emphasized in this chapter. The crystal inclination of nanosheets also has been investigated with the similarity of NSFETs with dissimilar metal gates. NSFETs can be scaled down continuously up to 5 nm or below nearby values without short-channel effects. At sub-5 nm technology quantum mechanical effect becomes severe. Below the 5 nm technology node, the NSFET similarity with dissimilar metal gates in the configuration of gate stack technology permits the tuning of its threshold voltage, which successively fascinates the research community concerning these circuits. For power management and better performance, NSFETs give the stretchability of breadth adaptation to circuit/device creators, because Fin-pitch does not restrict the effective breadth of nanosheets in NSFETs along with Fin quantization [36–38].

A DD model is presented for the characterization and investigation of NSFETs. This model included the BG-BC representation, the GDOS, which takes into consideration the energetic disorder and site density commonly associated with the organic materials, in addition to the PF mobility for small molecules. This analysis is extended for the comparison with the experimental measurements. Depending on the device's operating conditions, we conclude that more than one scenario is required to obtain a good fit. At low gate voltage values, both bulk and interface traps were found to be significant. At high voltage values, the voltage-current characteristics are very well described with the influence of fixed charges. The effects that are interface and bulk traps and fixed charges were investigated individually. It was followed by the transistor performance parameters extraction [2].

8.6 FUTURE PERSPECTIVES

In the future, NTs are poised to become one of the best-preferred choices for the smaller-sized devices of the next generation. For future device power consumption, the rising importunity for enlarging voltages embellishes an unquestionable confrontation that focuses on the rapid advance of the Internet of Things (IoT) and artificial intelligence chip automation. Furthermore, it can be concluded that NSFETs are the emerging contenders for subsequent applications of analog/digital consolidated circuits. An induced tunneling field effect transistor is combined for the nanosheet design, which address the future demand for low-power and high-performance computing applications and proposes the nanosheet structure featuring a high I_{ON}/I_{Off} current with a vertically stacked design [38,39]. The core-insulator-embedded NSFETs exhibit enhanced direct-current performance. The buried power rail (BPR) is an interesting proposal in the field of power delivery. Moreover, to ensure the improved short-channel effect prevention, the core-embedded NSFETs exhibit better electrostatic gate control, which is evidenced by a reduced off-current and steeper subthreshold slope. An inherent increment in an interface trap density with the additional interfaces in the core embedded NSFETs does not significantly degrade the performance of the device when it is compared especially with the conventional NSFETs. Therefore, core-embedded NSFETs emerged as one of the best superior alternatives for the semiconductor device technologies of the next generation. These NSFETs are essential for the progression beyond the 5 nm technology node and offer a combination of reduced variability and enhanced performance [40–42].

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9 Advanced Electrostatics in Nanosheet Transistors for Enhanced Device Scaling

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9.1 INTRODUCTION

In the past decade, semiconductor electronics have primarily revolved around Fin Field Effect Transistor (FinFET) and gate-all-around (GAA) nanowire transistor technologies. However, with the industry's focus shifting toward nanosheet transistors, a new era in semiconductor development has emerged. Nanosheet transistors outperform FinFETs and GAA nanowire transistors owing to their smaller footprint, reduced power consumption, and enhanced speed [1]. With billions of transistors, modern processors represent some of the most sophisticated and intricate systems engineered to date. As consumer demand for smaller, high-performance devices continues to grow, increasing transistor density and enhancing processor performance are becoming critical goals. These objectives align with Moore's Law, which emphasizes the continuous downscaling of transistors. Recent advancements have highlighted nanosheet transistors for their ability to overcome the physical and fabrication limitations of FinFET technology, leading to significant improvements in device performance. As a result, nanosheet transistors are becoming a central focus in modern semiconductor technology [2,3].

Nanosheets and FinFETs are both advanced semiconductor technologies designed to improve transistor performance as devices shrink in size. A FinFET uses a three-dimensional structure where the channel is shaped like a fin, allowing the gate to wrap around the channel on multiple sides. This 3D gate structure enhances control over the current flow, reducing leakage and improving efficiency compared to traditional planar transistors [4]. In operation, when a voltage is applied to the gate, it controls the flow of electrons between the source and drain, turning the transistor on or off [5]. Nanosheets take this concept further by using ultra-thin layers of material stacked on top of each other in the channel, providing even more precise control over electron flow (Figure 9.1).

Nanosheets can be made from materials like silicon or other semiconductors and offer higher current drive, better scalability, and lower power consumption [6].

DOI: 10.1201/9781003543923-9

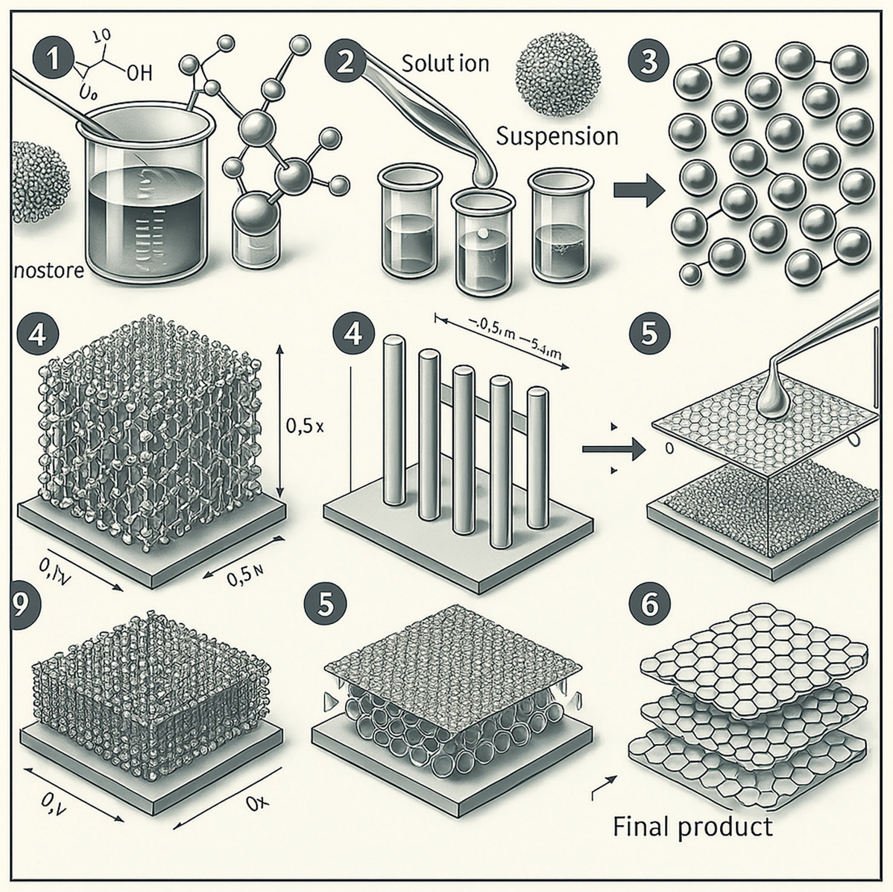

FIGURE 9.1 General working steps of fabrication of nanosheet.

In their working, the gate voltage controls the electron flow through the stacked nanosheets, further improving performance and enabling more efficient transistors in advanced electronic devices [7]. Both technologies aim to overcome traditional planar design limitations, enhancing modern semiconductor devices' overall performance (Figure 9.2) [4].

FinFET technology represents a significant breakthrough in the semiconductor field. Unlike conventional planar transistors, which use a flat gate and channel, FinFETs introduce a raised "fin" channel design, enhancing device density and reducing leakage power. This unique structure also offers a lower threshold voltage (V_{th}) and higher drive current compared to planar transistors, resulting in reduced circuit delay, minimized leakage, and improved overall performance while occupying less space and lowering the cost-per-unit of performance [8]. Nanosheet transistors, evolving from FinFET technology, provide further significant benefits by expanding channel widths within the same circuit footprint, they deliver increased drive current without increasing the overall size of the device [9] (Figure 9.3). With these

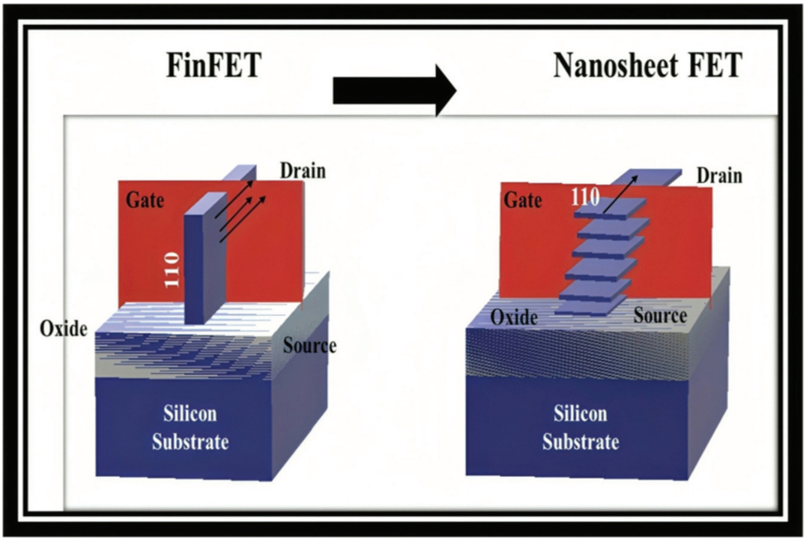
FinFET
Nanosheet FET
Drain
Gate
110
Oxide
Source
Silicon Substrate
Drain
Gate
110
Oxide
Source
Silicon Substrate

FIGURE 9.2 Nanosheet transistors originate from finFET technology [4].

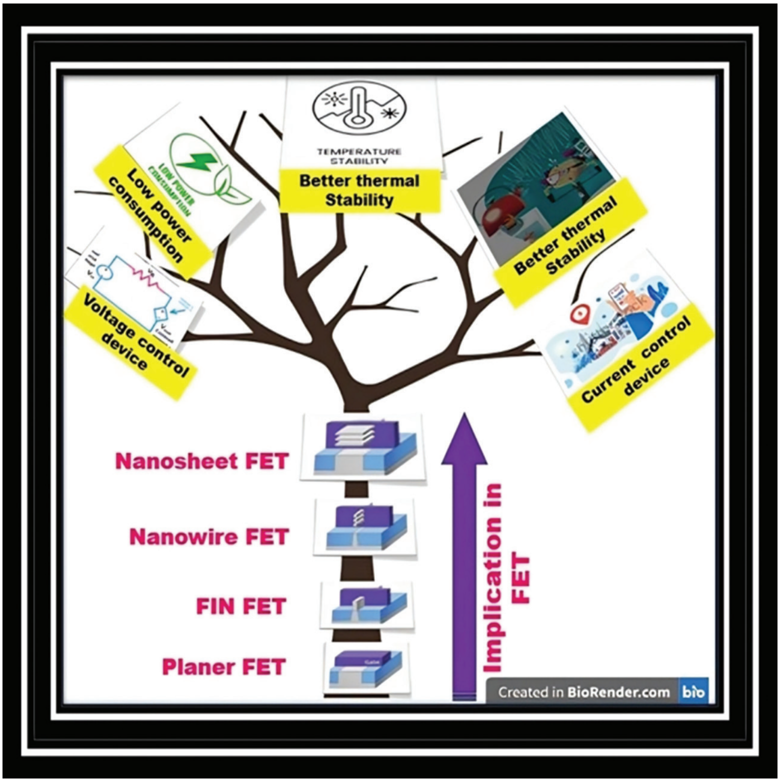
LOW POWER CONSUMPTION
Low power consumption
TEMPERATURE STABILITY
Better thermal Stability
Better thermal Stability
Voltage control device
Current control device
Nanosheet FET
Nanowire FET
FIN FET
Planer FET
Implication in FET
Created in BioRender.com

FIGURE 9.3 Implications and enhanced properties of nanosheet transistors.

advantages, nanosheet transistors are poised to become the preferred technology for the next generation of miniaturized devices, ensuring continued progress in semiconductor innovation. FinFETs were once considered the optimal technology for downscaling planar devices. With their shorter gate length, FinFETs offered improved gate-to-channel control and demonstrated strong performance at low voltages. However, as electronic design requirements evolved, FinFET technology struggled to keep pace [10,11]. Challenges related to layout, patterning, performance, and rising downscaling costs made FinFETs less suitable for modern circuits. The demand for increasingly taller and thinner structures in FinFETs became a major obstacle to further downscaling and performance improvements [12].

Nanosheet transistors, also known as GAA, multi-bridge channel, or nanobeam transistors, represent an advancement over FinFET technologies [13]. While nanosheet transistors are derived from FinFET technology, they provide significant advancements in FinFETs. Nanosheet transistors exceed the enduring power density ceiling of 100 W per square centimeter, the industry benchmark for the past decade. They advance integrated circuits' power and energy potential beyond what FinFETs technology can achieve. Nanosheet transistors are emerging as promising alternatives to FinFETs, especially for technology nodes below 5 nm. Unlike FinFETs, which face limitations in further scaling due to restrictions in fin height and fin pitch, nanosheet transistors use horizontally stacked sheets with improved control over these dimensions [14–16]. The sheet-to-sheet spacing, which is comparable to fin pitch in FinFETs, is determined by epitaxial processes rather than lithography, allowing for more precise scaling. This architectural shift enhances performance, scalability, and power efficiency, making nanosheet transistors well-suited for advanced semiconductor technology [17]. Nanosheet transistors offer improved device width per footprint by stacking multiple sheets vertically, unlike FinFETs, which utilize multiple fins arranged horizontally. This vertical stacking allows for greater effective width in a compact space. Additionally, nanosheet transistors provide enhanced gate control compared to FinFETs, which reduces short-channel effects. This improved control makes nanosheet transistors highly beneficial not only for logic applications but also for radio frequency (RF) circuits, as they deliver better performance and scalability at smaller nodes [18].

The chapter provides a comprehensive overview of nanosheet transistors. It explains their importance and addresses the limitations of FinFETs at very small technology nodes. It covers the basics of nanosheet transistors, including their structure, design, material properties, and manufacturing process. The chapter also discusses the charge transport mechanism, comparing the performance of nanosheet transistors with traditional transistors. Additionally, it also examines the applications of nanosheet transistors across diverse fields, including electronics, computing, and sensing technologies, highlighting their innovation potential.

9.2 FUNDAMENTAL OF NANOSHEET TRANSISTORS

Nanosheet transistors mark a significant advancement in semiconductor technology, distinguished by their extremely thin, two-dimensional (2D) structures. Nanosheet transistors utilize quantum confinement effects within their thin channels, enhancing charge transport and increasing carrier mobility. Their capacity to combine miniaturization with high-performance positions them as a key technology for future electronics.

9.2.1 BASIC STRUCTURE AND DESIGN

Nanosheet transistors feature ultra-thin semiconducting layers, or nanosheets, offering superior electrostatic control. Unlike FinFETs, their GAA design provides more accurate regulation of charge carriers, minimizing leakage currents and enhancing switching performance. Recent designs emphasize multi-layer nanosheet stacks, allowing for adjustable effective channel width to enhance performance in advanced technology nodes (below 5 nm) [19]. Major improvements involve refining gate length scaling and optimizing channel doping to sustain performance at reduced size. Nanosheet transistors present several benefits over FinFETs, largely thanks to their GAA architecture that delivers improved electrostatic control, lowering leakage currents and boosting performance at smaller dimensions. Their stacked, ultra-thin channels enable adjustable channel widths, allowing for more efficient power and performance optimization [20].

9.2.2 MATERIAL PROPERTIES

9.2.2.1 Semiconducting Material

Traditional silicon-based nanosheets provide excellent carrier mobility, recent research is investigating alternative materials such as silicon-germanium. These materials offer high mobility and adjustable bandgaps, making them well suited for exploiting quantum confinement effects at the nanoscale [21].

9.2.2.2 Quantum Mechanical Effect

Nanosheet transistors exhibit quantum confinement within their ultra-thin channels, which improves charge transport properties. Their distinctive two-dimensional structure reduces scattering and boosts carrier mobility [22].

9.2.2.3 Surface and Interface Properties

Effective design of the oxide-semiconductor interface is vital for reducing interface states that can capture charges and negatively impact performance. Additionally applying strain engineering can boost mobility in nanosheet transistors [23].

9.2.2.4 Bandgap Tunability

Materials like transition metal dichalcogenides (TMDs) offer adjustable bandgap through changes in layer thickness or chemical modification. This flexibility enables precise manipulation of the electronic properties of the nanosheets, making them adaptable for various applications [24].

9.2.3 FABRICATION TECHNIQUES

9.2.3.1 Chemical Vapor Deposition (CVD)

Chemical vapor deposition (CVD) is commonly employed for nanosheet growth because it can produce high-quality uniform thin films over areas. Recent advancements have facilitated the precise modulation of thickness and doping concentrations, which are critical for optimizing the performance of nanosheet transistors [25].

9.2.3.2 Molecular Beam Epitaxy (MBE)

It offers atomic-level precision, making it an ideal technique for fabricating heterostructures and superlattices in nanosheet transistors. The techniques are precious in a research setting, emphasizing experimental devices utilizing innovative materials such as TMDs [26].

9.2.3.3 Lithography and Etching

Advanced lithographic techniques, such as extreme ultraviolet (EUV) lithography, are employed to pattern nanosheet transistors with high precision. Subsequently, etching processes are implemented to define the nanosheet morphology and establish the requisite channel dimensions. These techniques are essential for achieving next-generation devices' precise feature sizes [27].

Thus, this can be termed the simplest explanation of the material properties and the fabrication techniques of nanosheet transistors, as shown in Figure 9.4.

9.3 CHARGE TRANSPORT MECHANISMS

Nanosheet transistors, a variant of field effect transistors (FETs), utilize ultra-thin semiconductor materials, such as molybdenum disulfide (MoS_2) or graphene, for their channel [28]. The charge transfer mechanisms in these devices are intricate and influenced by multiple factors, including the chosen materials, the device design, and the operating conditions [29]. A primary charge transfer mechanism in nanosheet

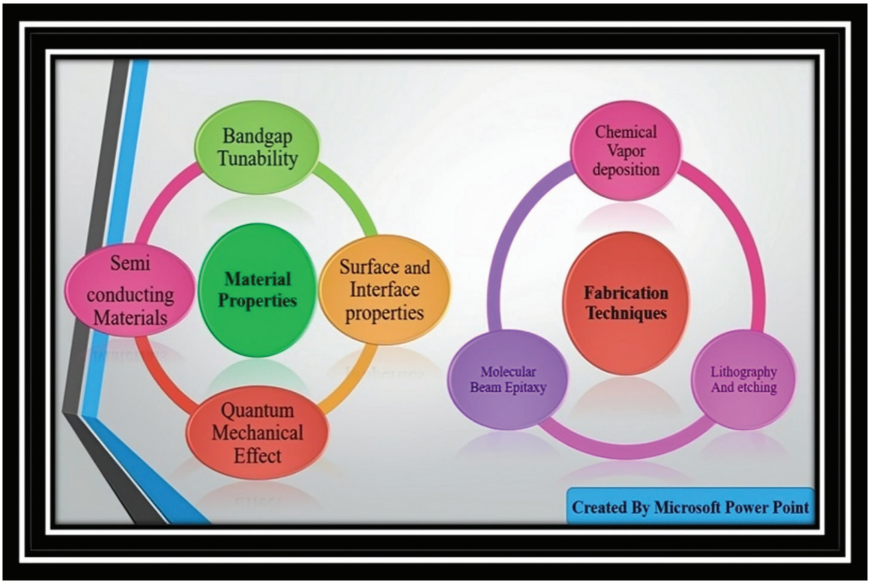
Bandgap Tunability
Semi conducting Materials
Material Properties
Surface and Interface properties
Quantum Mechanical Effect
Chemical Vapor deposition
Fabrication Techniques
Molecular Beam Epitaxy
Lithography And etching
Created By Microsoft Power Point

FIGURE 9.4 Material properties and fabrication techniques of nanosheet transistors.

transistors is the field effect, where an electric field applied between the gate and source terminals adjusts the conductivity of the channel. This modulation facilitates the control of current flow between the source and drain by adjusting the gate voltage. In MoS_2 nanosheet FETs, research indicates that electron transport predominates, while hole transport plays a relatively minor role [30,31]. Another key mechanism involves the transfer of hot charge carriers generated by light adsorption on plasmonic nanostructures that are attached to the nanosheets [32]. The charge transfer can also be affected by the introduction of molecular species such as ferrocene, which can permanently alter the electrical properties of the nanosheet, switching its behavior from ambipolar to unipolar. This effect is due to the formation of charge transfer complexes between the ferrocene and the semiconductor. In core–shell nanosheet structures, like ZnS-coated CdSe nanosheets, the shell can serve as a tunneling barrier for electron and hole transfer, thereby reducing their rates and enhancing charge separation efficiency [33,34].

9.3.1 EXPERIMENTAL OBSERVATIONS

9.3.1.1 5-nm Node Silicon Nanosheet Transistors

A study examines the effects of temperature on the performance of 5-nm node silicon nanosheet transistors. As the temperature rises from 250 to 450 K, critical performance metrics such as transconductance (gm) decrease from 228 to 200 μS, and the cutoff frequency declines from 568 to 524 GHz. Furthermore, the gm/IDS ratio deteriorates from 37.5 to 22.4/V, indicating that elevated temperatures reduce charge transport efficiency and degrade overall analog performance [35].

9.3.1.2 Multi-Nanosheet Transistor Exploration for Sub-3 nm Node

A study on mNS-FET devices showed that adding bottom oxide improved performance, with SS enhanced by 6.3%–17.6% and drain induced barrier lowering by 31.3%–59.9%. It also reduced gate capacitance, leakage current, and overall capacitance by up to 50.65%, while intrinsic resistance decreased by 15%. Circuit analysis confirmed reduced power consumption, though the “Bottom” structure exhibited less favorable characteristics compared to the “top” and “center” configurations [36].

9.3.1.3 Nanosheet Transistors for Neuromorphic Engineering

A study exploring the application of nanosheet transistors in neuromorphic engineering highlighted their potential by constructing two neuron models: the conventional Axon Hillock and a proposed alternative. Nanosheet transistors demonstrated remarkable sensitivity to femtoampere-range synaptic currents, producing diverse spike patterns with ultralow power consumption, thereby outperforming GPDK 45 nm transistors. These transistors show considerable promise for energy-efficient, scalable neuromorphic architectures, offering benefits in terms of compactness, integration density, and the potential for advanced neuromorphic memory systems, driven by high-speed access, low power consumption, and non-volatile properties [37].

9.3.1.4 SOI Nanosheet and Fishbone Transistors

This study explored the low-temperature electrical and quantum characteristics of SOI-stacked nanosheet (NS) and fishbone transistors. NS devices showed improved switching and off-state leakage at 6 K, with a linear decrease in threshold voltage above 50 K and quantum ballistic transport at ultralow temperatures. Fishbone FETs exhibited similar electrical behavior but poorer quantum transport due to SiGe fin channels. A hybrid simulation improved quantum characteristics by adjusting channel material ratios [38].

9.3.2 COMPARISON OF NANOSHEET TRANSISTORS WITH TRADITIONAL TRANSISTORS

Nanosheet transistors mark a major advancement in semiconductor technology compared to traditional transistors, especially in performance, size, and power efficiency. The following is a detailed comparison of nanosheets and traditional transistors, highlighting their structures, benefits, and challenges [39,40].

1. Planar transistors have limited design flexibility, while FinFETs offer improved flexibility, and nanosheet transistors provide high flexibility with adjustable channel width.
2. Nanosheet transistors are suitable for technology nodes beyond 5 nm, while traditional transistors are mainly used for older nodes.
3. Planar transistors are older technology, FinFETs are used in current technology, and nanosheet transistors are the main choice for 3 nm and smaller nodes.
4. Planar transistors have less effective electrostatic control, FinFETs have control, and nanosheet transistors offer superior control.
5. Planar transistors are less common in advanced applications, FinFETs are widely used, and nanosheet transistors are mainstream for TSMC and Samsung.
6. Nanosheet transistors are compatible with existing FinFET fabrication processes, whereas traditional transistors use older processes.

9.4 APPLICATIONS AND INNOVATIONS OF NANOSHEET TRANSISTORS

9.4.1 IN ELECTRONICS AND COMPUTING

Nanosheet transistors are paving the way for a new era in electronics and computing, offering superior performance, reduced size, and improved power efficiency over conventional silicon-based devices [41]. In electronics, nanosheets are being integrated into FETs to improve device scalability, allowing manufacturers to push the limits of Moore's Law by shrinking transistor size while maintaining functionality [42]. Nanosheet transistors provide superior electrostatic control over the channel, which reduces short-channel effects and power leakage, key concerns in current semiconductor technologies. These features make them a prime candidate for next-generation high-performance processors, memory devices, and integrated circuits [43]. Their use in computing is also expected to drive innovation in quantum computing, where smaller, faster transistors can accelerate processing speeds while lowering energy consumption. Nanosheet-based chips will likely be incorporated into devices enabling faster, more energy-efficient computing solutions [44].

9.4.2 SENSOR TECHNOLOGIES

Nanosheet transistors are revolutionizing sensor technologies due to their high sensitivity and tunability. They can be used in developing biosensors, chemical sensors, and environmental monitoring devices [45]. The unique properties of nanosheet transistors—such as high surface-to-volume ratios and low power consumption—allow for more accurate detection of molecular-level changes in a system [46]. In medical diagnostics, nanosheet-based sensors can detect biomolecules, such as proteins or DNA, at ultralow concentrations, making them invaluable for early disease detection. The increased surface area of nanosheets enhances the interaction between the sensor and the analyte, enabling real-time monitoring of biological processes [47]. In environmental applications, these sensors can be used to detect toxic gases, pollutants, or hazardous chemicals in the air and water, ensuring safer environments by providing quick alerts when dangerous levels are reached [48]. Nanosheet-based sensors are also finding applications in wearable electronics for continuous health monitoring, adding a new dimension to personalized healthcare [49].

9.4.3 OTHER EMERGING APPLICATIONS

The versatility of nanosheet transistors opens doors to several other emerging fields. In energy storage and conversion, nanosheet-based transistors can be integrated into lithium-ion batteries and fuel cells to enhance charge transport and improve energy efficiency [50]. These materials offer advantages in energy harvesting, storage, and delivery, contributing to the development of more sustainable energy systems [51]. In the optical and photonic industries, nanosheets can be used to develop high-speed photodetectors and light-emitting devices for advanced communication systems. Nanosheet materials like 2D TMDs are being explored for their potential in flexible electronics, leading to innovations in foldable phones, wearable technology, and bendable displays [52]. Nanosheets are becoming critical components in neuromorphic computing and artificial synapses, where they mimic the operation of human neurons [53]. Table 9.1 summarizes the performance and application characteristics of different nanosheet transistors.

9.5 CHALLENGE AND PROSPECTS

9.5.1 TECHNICAL CHALLENGE

9.5.1.1 Material Limitations

Due to their ultra-thin nature, nanosheet transistors are susceptible to interface defects between the nanosheet and the substrate, which can negatively impact performance. Variations in material quality, including surface roughness or impurities,

TABLE 9.1
Performance and Applications of Various Nanosheet Transistors

Material Used	Device Type	Performance Benefits	Application Field	References
5 nm node N-channel nanosheet transistor (NST)	Nanosheet transistor	Output conductance increases with temperature, early voltage improves with temperature, and discharge time improves with temperature	Analog applications	[35]
10 nm junctionless nanosheet FET with high K-gate stack	Junctionless nanosheet FET	Cutoff frequency in THz range, analog/RF performance parameters less sensitive to temperature variations, lesser power consumption at extremely scaled LG	Nano-electronics	[54]
MoS_2, Al_2O_3, HfO_2, AlO_x	Symmetric and asymmetric MoS_2 nanosheet transistors	Subthreshold swing, drain-induced barrier lowering, current density	Low-power applications as per the international roadmap for devices and systems (IRDS)	[55]
Silicon	Vertically-stacked silicon nanosheet FETs	Reduced short-channel effects, minimized leakage for scaling beyond FinFETs at 3 nm	–	[56]
ZnO nanowires, ZnO nanosheets	Field effect transistors (FETs), source-gated transistors (SGTs)	SGTs offer bias stress robustness and stability than FETs	AMOLED display circuits	[57]

can cause instability in charge transport [58]. When nanosheets reach atomic-scale thickness, quantum confinement effects become prominent. Although these effects can improve performance, they also introduce complexities in device behavior at the nanoscale, making precise control more difficult [59]. Nanosheet transistors frequently encounter challenges with heat dissipation because of their small size and compact structure [60].

9.5.1.2 Fabrication Difficulties

Although methods such as CVD and MBE have advanced considerably in nanosheet fabrication, scaling these techniques for industrial use is difficult, Achieving uniform thickness and large-scale production are major obstacles [61]. Patterning ultra-thin nanosheets demands great precision to prevent material damage or the introduction of defects. High-resolution lithography and etching techniques must be further improved to efficiently produce nanosheet transistors [62].

9.5.2 ENVIRONMENTAL AND ECONOMIC CONSIDERATION

9.5.2.1 Environmental Impact

Nanosheet transistors commonly utilize materials such as rare earth metals and TMDs, but the environmental challenges associated with their extraction and processing could affect the sustainability of future production. The fabrication process, particularly with high-precision techniques like CVD, can produce substantial material waste. Managing waste and recycling semiconductor material is crucial to reducing environmental harm [63].

9.5.2.2 Economic Feasibility

The sophisticated fabrication methods needed for nanosheet transistors, like MBE and CVD, are costly. With increasing demand for smaller, high-performance devices, developing more affordable manufacturing processes will be essential for making these transistors commercially feasible. The materials essential for nanosheet transistors, like high-purity transition metals, face supply chain constraints, Variations in material availability could drive up costs and hinder the widespread adoption of this technology globally [64].

9.5.3 CONCLUSION

Nanosheet transistors signify a groundbreaking shift in semiconductor technology, merging high-performance capabilities with the potential for transformative applications. Their ability to support advanced charge transport mechanisms, paired with innovative design options like 3D stacking and multifunctional integration, positions them as pivotal components in the evolution of electronic devices. While current challenges persist in terms of integration, stability, and environmental durability, ongoing research and development promise to overcome these barriers. As efforts to refine fabrication techniques and explore novel materials continue, nanosheet transistors are anticipated to play a central role in enabling next-generation, high-density, and low-power electronic systems.

9.5.4 FUTURE RESEARCH DIRECTION

Ongoing research into two-dimensional materials like MoS_2 and WS_2 is vital for enhancing the performance of nanosheet transistors. While these materials possess outstanding electronic properties, their integration with existing fabrication technologies remains early. Researchers are studying materials with topologically protected edge states, which could result in transistors that offer better charge transport and reduced power usage [65]. The stacking of nanosheet transistors into three-dimensional structures is gaining attention as a promising area of research. This technique could transform device miniaturization and allow for higher transistor densities in next-generation semiconductor technologies. Integrating nanosheet transistors with technologies like quantum dot arrays or photonic systems could new opportunities for creating multifunctional devices that extend beyond conventional electronic uses [66]. To guarantee long-term device reliability, additional research is required to tackle problems related to stability across different environmental conditions, such as temperature and humidity. There is increasing interest in a material capable of self-repairing minor defects, which could enhance the durability and dependability of nanosheet transistors in challenging operating conditions [67]. To sum up, nanosheet transistors represent a major leap forward in semiconductor technology, providing outstanding performance and new possibilities for miniaturization. Their unique structural and material characteristics enhance charge transport and open doors to novel applications in various areas. With ongoing research addressing current issues and exploring new materials and fabrication approaches, nanosheet transistors are likely to be integral to the advancement of future electronic devices and systems.

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10 The Charge Transport of the Breast Cancer Cells on Metal Strip-Loaded Extended Source-TFET Biosensor

Madhulika Verma and Sachin Agrawal

10.1 INTRODUCTION

Cancer encompasses a wide variety of diseases characterized by the uncontrolled growth and spread of atypical cells. If these cells are not managed effectively, they can lead to severe consequences, including death. There are over 100 distinct types of cancer, each capable of originating in any tissue within the body. The development of cancer may be attributed to genetic mutations, environmental exposures, or a combination of these factors [1].

One common form of cancer is breast cancer, which originates from atypical cell growth in the breast tissue. Typically, these cancer cells begin in the milk ducts or lobules and grow uncontrollably, forming a tumor that may eventually metastasize to other parts of the body [2]. The classification of breast cancer is based on specific characteristics of the cancer cells, such as the presence of hormone receptors and the levels of the HER2 protein. These factors are crucial to find the type of breast cancer and guiding appropriate treatment strategies [3,4].

Breast cancer cells (BCC) are divided in two categories: healthy and cancerous cells. Non-tumorigenic cell lines, such as MCF-10A, consist of immortalized, non-cancerous breast epithelial cells that are often utilized to model healthy breast tissue. On the other hand, cancerous breast cell lines such as HS578t, MDA-MB-231, MCF7, and T47D represent various forms of breast cancer. HS578t and MDA-MB-231 are classified as triple-negative breast cancer (TNBC) cell lines. In contrast, MCF-7 and T47D are hormone receptor-positive lines that express estrogen receptors, with MCF-7 also expressing progesterone receptors. This makes them responsive to hormone-based therapies [5].

Nowadays fast detection and curing have significantly improved, but breast cancer remains a major global health issue [6]. Various diagnostic methods have been employed to detect breast cancer, each with its own set of limitations. Clinical Breast Exams (CBE) can identify lumps, but may overlook smaller or deeper tumors.

DOI: 10.1201/9781003543923-10

Mammography is an effective screening tool, but sometimes it yields false positive or negative results, particularly in women with dense breast tissue. Ultrasound is valuable for further examination, but it could face issues to differentiate between benign and malignant lesions [7,8]. MRI provides high-resolution images; however, it is costly and sometimes results in false positives, leading to unnecessary biopsies. Biopsies are essential for confirming a diagnosis but can be risky due to infection. Histopathological analysis of biopsy samples is crucial for diagnosis however, limited by the representativeness of the sample. Genetic testing identifies the inherited risk factors though it cannot be performed frequently due to its complexity and expense. Hormone Receptor and HER2 Testing are vital for treatment planning, but sometimes may produce ambiguous results. Due to these limitations, there is a huge demand for novel diagnostic approaches for BCC molecules [9,10].

In recent research, various biosensor devices have been developed to leverage the neutral and charged properties of BCC molecules. These devices include field-effect transistors (FETs), carbon nanotube FET, graphene-based FET, fin-FET, tunnel FET (TFETs), ferroelectric-TFETs, polarity control-TFETs, and MoS_2 channel-based TFET biosensors [11–18]. Researchers have investigated the neutral properties of BCC biomolecules (e.g., MCF-10A as healthy cells and HS578t, MDA-MB-231, MCF7, and T47D as cancerous cells) across a frequency range of 200 MHz to 13.6 GHz [19,20]. These cell lines are instrumental in cancer research. High electron mobility transistors (HEMTs) have also been identified as effective devices for breast cancer detection [21,22].

This book chapter introduces a novel sensor device named as the dual-metal double-gate metal strip-loaded extended source-Tunnel FET (MS-ES-TFET) designed for the finding of BCC. The device features a metal strip and a germanium/silicon heterojunction that enhance tunneling at the active junction [23,24]. Additionally, the extended source increases the tunneling area [25], while the double-gate configuration improves the electrostatic field in the channel [26]. Consequently, the device performance is enhanced for detecting the BCC. The dual-metal design incorporates two different metals at the gate electrodes, labeled M1 and M2. Metal M1 improves the ON-drain current (I_{ON}), on the other hand metal M2 reduces the OFF-drain current (I_{OFF}), which is highly essential for the device [27].

10.2 DEVICE STRUCTURE

The metal strip-loaded extended source-TFET (MS-ES-TFET) biosensor employed the charged plasma method (CPM) for doping, as illustrated in Figure 10.1. This method effectively reduces Random Dopant Fluctuation (RDF), which typically arises due to the small number of dopants in semiconductor devices, and also simplifies the fabrication process [28]. The use of a germanium/silicon heterojunction enhances the abruptness at the active junction, while the metal strip further sharpens this junction by forming n^+ pockets in the adjacent silicon body.

The extended source design provides a larger area to drive current through tunnel both along and across the axes of the device [29]. In simulations, the MS-ES-TFET biosensor is modeled on a 20×32 nm² intrinsic substrate, with the channel, source, and drain length

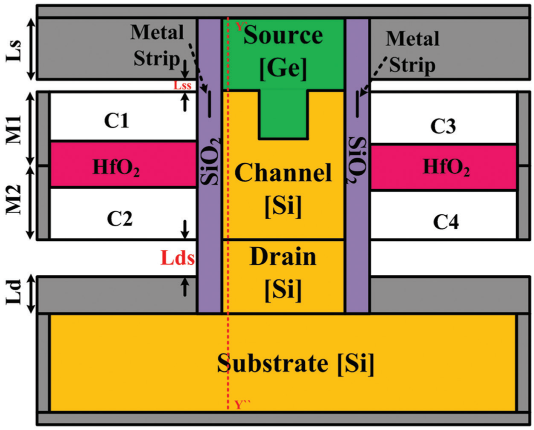

FIGURE 10.1 Schematic diagram of metal strip-loaded extended source heterojunction TFET (MS-ES-HJ-TFET) biosensor device.

of 30, 12, and 10 nm, respectively. Spacers of 3 and 5 nm are used at the source and drain to ensure proper isolation. The body thickness is set to 10 nm, corresponding to the Debye length. The extended source region is considered to be 10 nm × 4 nm.

To prevent leakage currents, silicon dioxide (SiO_2) also known as native oxide is used as the isolation layer. The electrostatic field in the channel is controlled by dual gate materials, M1 and M2, of work functions 4.2 and 5.1 eV, respectively. It enhances the device performance and ensuring efficient charge control.

To detect BCC biomolecules, four nano-gap cavities, labeled C1, C2, C3, and C4, are etched into the HfO_2 oxide layer. Each cavity is of 10 nm in length and 10 nm in thickness, which is sufficient to capture the cancer biomarker. Further, a metal strip with a 3.9 eV work function is placed in the native oxide adjacent to cavities C1 and C3 to enhance the tunneling effect.

Proper doping is crucial for the TFET device to achieve the desired performance. To accomplish this, platinum ($\varphi_{Pt} = 5.93$ eV) is employed on the source side to produce a hole plasma, as its work function is greater than that of silicon. On the drain side, hafnium ($\varphi_{Hf} = 3.9$ eV) is used to create an electron plasma, as its work function is lower than silicon. This strategic doping configuration ensures efficient device operation by optimizing the charge transport in both the source and drain regions.

10.2.1 IMMOBILIZATION MECHANISM OF BIOMOLECULES (CHARGE TRANSPORT)

The biospecies of BCC are first immobilized within four nano-gap cavities. These biospecies then interact with the bioreceptor on the device, triggering a biological response. This response is transmitted to the TFET transducer, which converts it into an electrical signal. In the final stage, the sensor's reader amplifies, processes, and displays the output [30].

Biomolecules can be detected in two ways: through neutral biomarkers or charged biomarkers. Neutral biospecies exhibit specific dielectric properties, allowing the detection of their permittivity based on the device's electrical characteristics. In contrast, charged biomarkers are detected by measuring charge densities, which influence the electric characteristics.

Healthy and cancerous breast cells display various neutral biospecies at a frequency of 230 MHz, including MCF-10A ($k = 4.5$), HS578t ($k = 22$), MDA-MB-231 ($k = 24.5$), MCF7 ($k = 27.5$), and T47D ($k = 32$) [20]. The response of these biospecies is observed by immobilizing them in the C1, C2, C3, and C4 cavities of the dual-metal double-gate MS-ES-TFET biosensor.

The negative charge has found on normal and cancerous breast cells surface [31]. The charge densities for these cells when used in the MS-ES-TFET device are considered to be -1×10^{10}, -1×10^{11}, and $-1 \times 10^{12}/\text{cm}^2$. The varying charge densities have a crucial role in influencing the device's sensitivity to different cell types and help TFET biosensor to detect and differentiate between normal and cancerous cells [17].

10.2.2 Simulation Model

The proposed MS-ES-TFET biosensor designed through Silvaco (ATLAS) tool using several key models to accurately represent its behavior [32]. The band-to-band tunneling (BTBT) model is fundamental in describing the quantum tunneling of the carriers. This is often estimated using the Wentzel-Kramers-Brillouin (WKB) approximation to evaluate tunneling probabilities. For carrier recombination, both the Shockley–Read–Hall (SRH) and Auger recombination models are applied, as they help in understanding leakage currents and carrier lifetimes, especially in high doping regions. Fermi–Dirac statistics are also essential, providing a quantum mechanical perspective on carrier distribution, which is particularly significant for heavily doped regions. Additionally, trap-assisted tunneling (TAT) is included to capture leakage currents caused by defects that offer intermediate tunneling pathways.

In terms of numerical techniques, the Newton–Raphson method (often referred to as the Newton trap method) is used to solve complex nonlinear equations in the simulation of MS-ES-TFET biosensors [32]. This iterative approach is essential for approximating solutions related to carrier transport and quantum tunneling, accounting for effects such as tunneling and trap-assisted processes, while maintaining accuracy in the presence of quantum effects.

10.3 RESULT AND DISCUSSION

To detect cancer cell biomarkers, a suitable supply voltage is essential. When this voltage is applied, it induces variations in the electrical characteristics of the biomarkers, which can be analyzed using both DC and RF analysis. These variations provide critical insights into the behavior of the biomarkers, enabling the detection and differentiation of cancerous cells from healthy ones based on their unique electrical responses. This voltage-controlled analysis forms the basis for sensitive and accurate biosensing in the device.

10.3.1 DC ANALYSIS

To analyze carrier concentration, energy band engineering and electron (e^-) tunneling rates in the proposed device, a 1 nm Y′–Y″ cutline is placed at the native oxide/silicon interface. These characteristics are studied for different neutral BCC biomarkers by filling the nano-cavities with dielectric constants (k) of 1, 4.5, 22, 24.5, 27.5, and 32.

Figure 10.2a illustrates the carrier concentration response along the device's y-axis with varying cancer cell dielectric constants. As the neutral charged of the biomolecules increases, the hole concentration in the source region rises, suppressing the e^- concentration. This is due to the platinum metal used for source doping, which creates a hole-rich environment. However, in the channel region the e^- concentration becomes higher than the hole concentration due to the V_{gs} of 2 V. As the permittivity of the cancer cells increases, the electron concentration also rises in the channel, especially under cavities C1 and C3, due to the increased capacitive nature. In the drain spacer region, the electron concentration rising continuously which corresponds to the higher capacitance in cavities C2 and C4, driven by the BCC biomolecules. The drain region has a higher electron concentration since it is doped with hafnium metal, which contributes to the overall electron-rich environment at the drain [33].

Figure 10.2b illustrates the ON state energy band diagram with different neutral biomolecules. As different permittivity of cancer biomolecules is introduced into the cavities, the increased band bending is observed at the active junction. For a permittivity of $k = 1$, the tunneling width is comparatively larger than other k-values. Conversely, at $k = 32$, the tunneling width is the smallest, resulting in sharper tunneling at the active junction. In the source region, both the conduction band and valence band shift upwards with increasing permittivity of the neutral biomolecules. This shift occurs because a higher k-value leads to increased hole concentration [34].

In Figure 10.2c, increasing the k-value rises the electron tunneling rate due to reduction in tunneling width [28]. The tunneling rate is measured in a semiconductor under the metal strip region. It varies across different biomarker samples: 30.5 for air, 31.0 for MCF-10A, 31.13 for HS578t, 31.14 for MDA-MB-231, 31.15 for MCF7, and 31.16 for T47D. For k-values of 22, 24.5, 27.5, and 32 biomarkers the tunneling rate variation is very small because in Figure 10.2b shows less deviation for these values. This similarity is attributed to the fact that these biomarker samples exhibit almost same tunneling width in their energy bands.

The I_{ds} versus V_{gs} curve of the MS-ES-TFET device with various BCC biomarkers are illustrated in Figure 10.3a, where I_{ds} increases with the k of the biomarker. This is because of improved coupling capacitance within the nano-gap cavity regions, which results in an enhanced tunneling rate [35]. Varying the k-value from 1 to 4.5, a significant enhancement in I_{ds} is observed, indicating a more efficient tunneling process. This is primarily due to the reduced effective tunneling barrier width and higher electron transmission probability across the active junction. However, as the dielectric constant reaches to higher values ($k = 22$, 24.5, 27.5, and 32), the increase in drain current becomes very less pronounced.

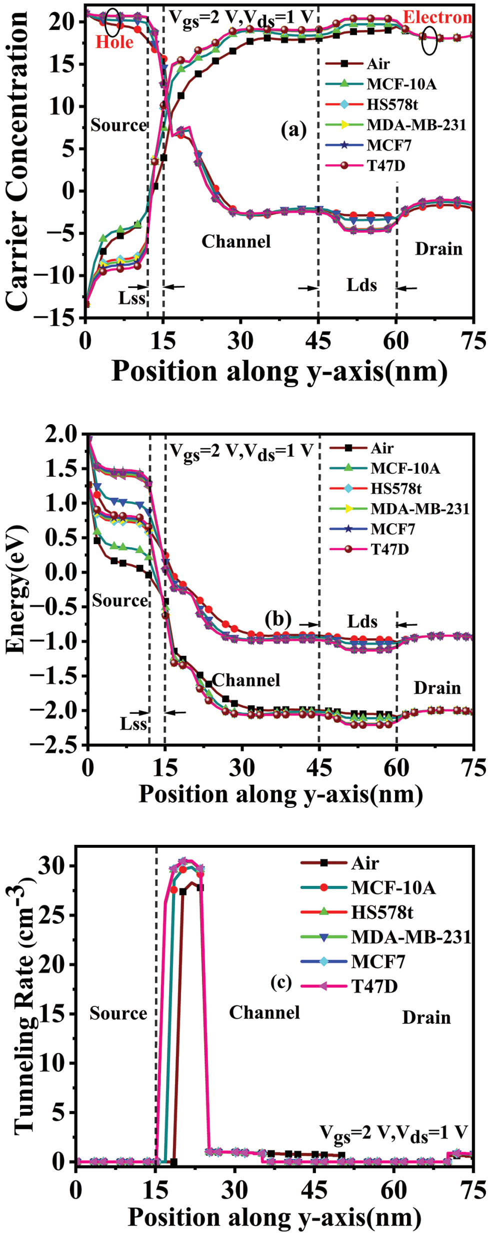

FIGURE 10.2 Plot of (a) carrier concentration, (b) energy and (c) electron tunneling rate with different BCC biomolecules under ON state.

In Figure 10.3b, the behavior of transconductance (g_m) of the proposed biosensor is graphed versus gate voltage for numerous dielectric constants ($k = 1$, 4.5, 22, 24.5, 27.5, and 32). Transconductance refers to the ratio of the variation in I_{ds} to the variation in V_{gs}, while maintaining a constant V_{ds} [17]. The graph reveals that g_m increases

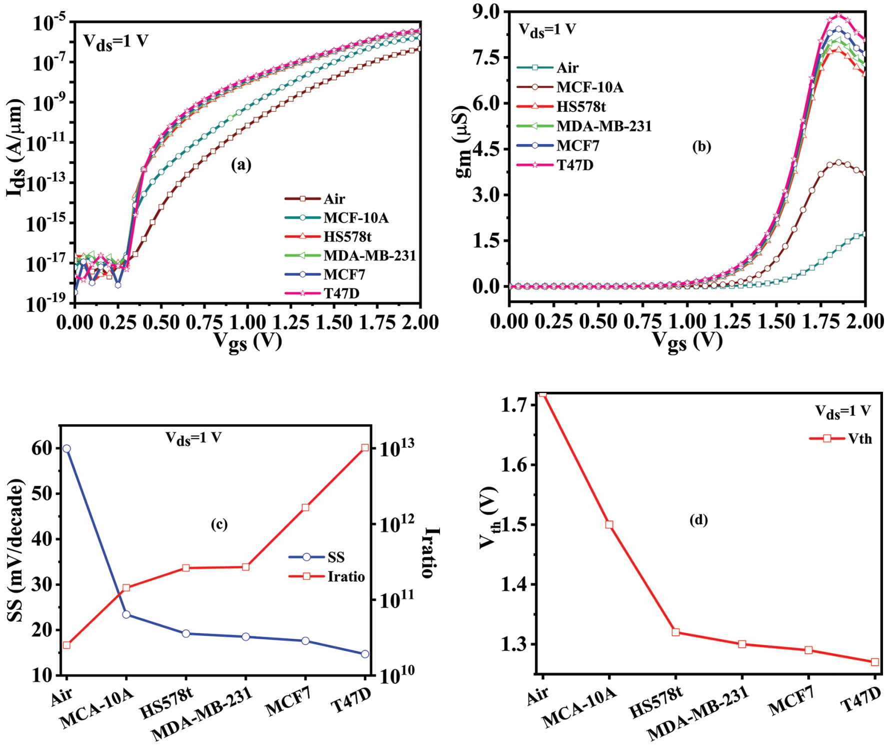

FIGURE 10.3 The plot depict (a) the drain current and (b) the transconductance as functions of gate voltage for various BCC molecules. Additionally, (c) shows the SS and I_{ratio} as they change with different cancer cell types, while (d) illustrates the threshold voltage in relation to breast cancer molecules at $V_{ds} = 1$ V for the MS-ES-TFET device.

gradually with dielectric constant, indicating improved device performance. This is because a higher dielectric constant enhances the electrostatic field over the channel, forwarding to more efficient modulation of the drain current. The highest g_m value is achieved at $k = 32$ (T47D). The improved transconductance at higher k-values is beneficial for detecting small changes in biomarker concentrations, making the device a good solution in biosensing consumption.

The subthreshold swing (SS) is inversely proportional to the subthreshold slope, defined as $d(V_{gs})/d(\log_{10}(I_{ds}))$ in mV/decade [36]. For optimal device performance, the SS should be low, as it indicates the steepness of the transfer characteristics. A lower SS tenders the fast switching speed of the device. Figure 10.3c illustrates the relationship between SS and the current ratio (I_{ratio}) for different BCC biomolecules. Here, one can notice that SS showing inverse relationship with k. The lowest SS value is observed at $k = 32$, reaching 14.7 mV/decade, which indicates improved switching behavior and better device performance at this dielectric constant.

The ON/OFF (I_{ratio}) current ratio is termed as a ratio of I_{ds} at $V_{gs} = 2$ V (ON state) and $V_{gs} = 0$ V (OFF state). This ratio indicates the device's ability to distinguish between ON and OFF states. A high I_{ratio} shows better performance, whereas, the low I_{ratio}

reveals a less distinct output swing between these two states [26]. From Figure 10.3c, it is clear that the current ratio (I_{ratio}) increases with dielectric constant of the cancer cell biomolecule. The highest current ratio of 1.02×10^{13} is obtained at $k = 32$, signifying strong ON/OFF current differentiation. This improvement further enhances the biosensor's capability to notice subtle changes in the biomolecule environment.

The threshold voltage (*Vth*) is the point where the proposed biosensor begins its transition, signifying the onset of device conduction. For optimal device performance a lower V_{th} is desirable as it allows the sensor to operate efficiently at lower voltages [37]. Figure 10.3d depicts the correlation between the threshold voltage and cancer cell biomolecules. As seen, by increasing the *k*-value, V_{th} decreases. This trend suggests that the device requires less voltage to switch on as the biomarker's dielectric constant rises, improving its sensitivity and performance in biosensing applications. The specific V_{th} values for different biomolecule dielectric constants are as follows: 1.72 V for $k = 1$, 1.5 V for $k = 4.5$, 1.32 V for $k = 22$, 1.3 V for $k = 24.5$, 1.29 V for $k = 27.5$, and 1.27 V for $k = 32$.

As the BCC exhibit negative charge (NC) on its surfaces, it is essential to examine its effect on the proposed device's performance [38,39]. The impact of negatively charged BCC biomolecules on the I_{ds}, V_{th}, and SS is analyzed under the conditions of $V_{\text{gs}} = 2$ V and $V_{\text{ds}} = 1$ V.

Figure 10.4a presents the Ids versus Vgs curve of the device for different negatively charged densities of BCC biomolecules. Increasing the negative charge density from $-1 \times 10^{12}\,\text{cm}^{-2}$ to $-1 \times 10^{10}/\text{cm}^2$, the drain current ($I_{\text{ds}}$) is enhanced. The decrease in I_{ds} occurs due to negatively charged biomolecules density decreases the number of available electrons in the channel and hence reducing the drain current.

Figure 10.4b illustrates the effect of NC biomolecule density on the threshold voltage (V_{th}) of the MS-ES-TFET biosensor. As the negative charge density increases, the threshold voltage decreases. At a charge density of $-1 \times 10^{10}/\text{cm}^2$, the proposed device starts conducting faster as compared to NC density of -1×10^{11} or $-1 \times 10^{12}/\text{cm}^2$ in nano-gap cavities. This signifies that lower NC densities lead to more efficient switching behavior. Figure 10.4c shows the subthreshold swing (SS) of the device as a function of NC biomolecule density. The SS improves with increasing negative charge density, indicating that the device's switching becomes steeper. A lower SS value corresponds to a more abrupt transition between the ON and OFF states. At $\rho = -1 \times 10^{10}/\text{cm}^2$, the device achieves a steep SS of 19.7 mV/decade, indicating superior switching performance and fast response to changes in gate voltage.

10.3.2 SENSING ANALYSIS

Sensitivity refers to a biosensor's capability to detect minimal changes in analyte concentration, serving as a key parameter for assessing the performance of the MS-ES-TFET biosensor. It is evaluated in comparison to air across various electrical parameters. The drain current sensitivity is calculated using a specified formula [40]:

$$S_{I_{\text{ds}}} = \frac{I_{\text{ds}}^{\text{BCC-bio}}}{I_{\text{ds}}^{\text{air}}} \tag{10.1}$$

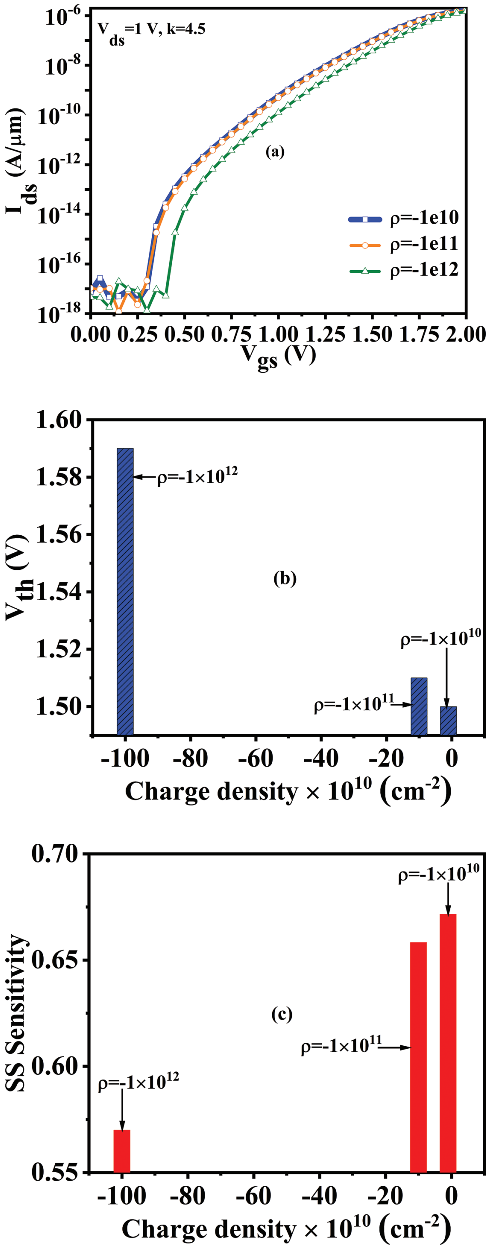

FIGURE 10.4 Impact of negative-charged densities on (a) transfer characteristics, (b) V_{th} and (c) SS with respect to MCA-10A (healthy) molecules at $V_{gs} = 2$ V and $V_{ds} = 1$ V.

The ratio of the I_{ds} when the cavity region contains healthy and cancerous cell biomarker ($I_{ds}^{BCC\text{-}bio}$) to the drain current when the cavities contain air (I_{ds}^{air}) is used to calculate the biosensor sensitivity.

In Figure 10.5a, the I_{ds} sensitivity ($S_{I_{ds}}$) improves with the existence of both healthy and cancerous cell biomolecules. This is due to improved drain current with BCC dielectric constant (*k*-values). The lowest and highest sensitivities are observed at $k = 4.5$ and 32, respectively. It indicating that the device becomes more responsive as the biomarker's *k*-value increases. Similarly, in Figure 10.5b the transconductance sensitivity (S_{gm}) improves with *k*-value. The S_{gm} expressed as [35]

$$S_{g_m} = \frac{g_m^{\text{BCC-bio}}}{g_m^{\text{air}}} \tag{10.2}$$

where $g_m^{\text{BCC-bio}}$ and g_m^{air} represent the transconductance when the nano-gap cavities contain BCC biomolecules and air, respectively. The transconductance sensitivity (S_{gm}) peaks only within the V_{gs} range of 0.25–1 V, while at other gate voltages, their sensitivity is zero. The highest transconductance sensitivity (4.2×10^3) is observed at $k = 32$, indicating the optimal performance of the biosensor in detecting biomolecules within this specific voltage range.

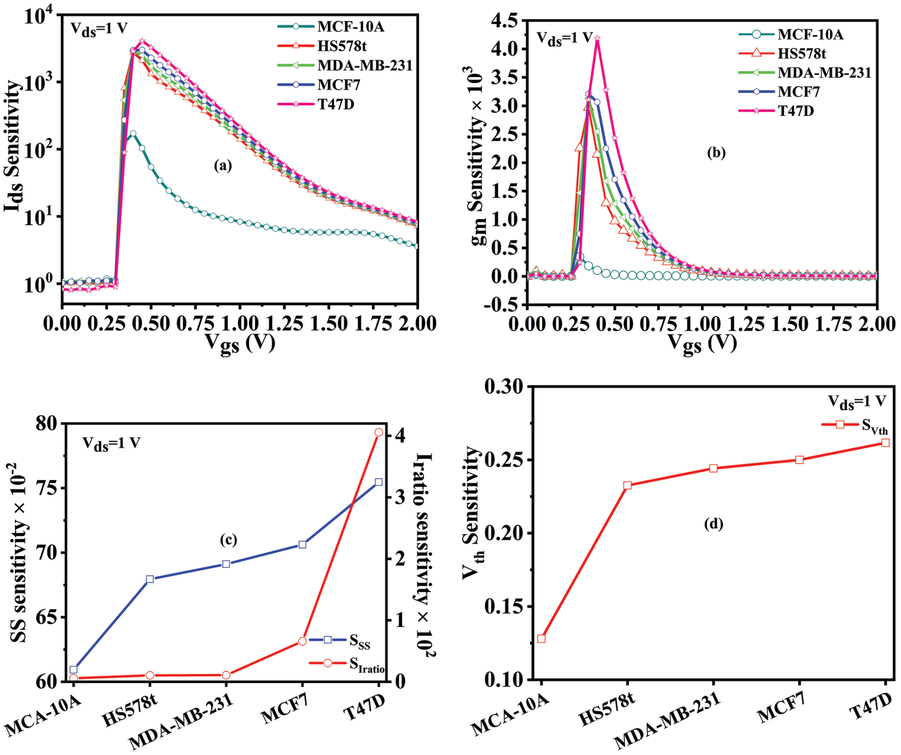

FIGURE 10.5 The sensitivity of (a) I_{ds} and (b) g_m characteristics along V_{gs} with numerous BCC molecules. (c) S_{SS} and $S_{I\text{ratio}}$ and (d) $S_{V_{th}}$ graph versus different BCC molecules at $V_{gs} = 2$ V and $V_{ds} = 1$ V.

The MS-ES-TFET biosensor's SS sensitivity (S_{SS}) is expressed as follows [41]:

$$S_{SS} = \left| \frac{SS^{\text{BCC-bio}} - SS^{\text{air}}}{SS^{\text{air}}} \right| \tag{10.3}$$

where $SS^{\text{BCC-bio}}$ represents the SS when BCC biomarkers are existing in the cavity region, and SS^{air} represent the SS when air molecules fill the nano-gap cavity. Figure 10.5c illustrates the S_{ss} of the MS-ES-HJ-TFET device. It indicates that SS sensitivity increases as the permittivity of cancer cell biomolecules rises. As seen, the device attains the S_{SS} of 0.61, 0.679, 0.69, 0.71, and 0.75 at $k=4.5$, 22, 24.5, 27.5, and 32 biomolecules, respectively. The same graph also displays the I_{ON}/I_{OFF} sensitivity ($S_{I_{\text{ratio}}}$) along different biomolecules. The below equation further quantify this relationship [42]:

$$S_{I_{\text{ratio}}} = \frac{I_{\text{ratio}}^{\text{BCC-bio}}}{I_{\text{ratio}}^{\text{air}}} \tag{10.4}$$

The I_{ON}/I_{OFF} sensitivity ($S_{I_{\text{ratio}}}$) is defined as the proportion of the I_{ratio} when the nano-gap cavities are filled with cancer molecules to the current ratio when the cavities contain no molecules. This sensitivity improves as different biomolecules are immobilized in the cavities. From the graph, $S_{I_{\text{ratio}}}$ values of 5.73, 10.47, 10.75, 65.73, and 405.57 are obtained for the respective healthy and cancerous molecules. These values demonstrate that the sensitivity rises significantly with the occurrence of BCC biomarker, highlighting its potential for accurate detection of cancer cells.

The threshold voltage sensitivity ($S_{V_{\text{th}}}$) can be evaluated using Equation (10.5). Here, $V_{\text{th}}^{\text{BCC-bio}}$ represents the threshold voltage when the nano-gap cavities contain biomolecules, and $V_{\text{th}}^{\text{air}}$ represents the threshold voltage when the cavities are empty (containing only air) [43]. This sensitivity measures the threshold voltage sensitivity of the device. The higher sensitivity indicates a greater influence of the biomolecules on the biosensor's switching behavior.

$$S_{V_{\text{th}}} = \left| \frac{V_{\text{th}}^{\text{BCC-bio}} - V_{\text{th}}^{\text{air}}}{V_{\text{th}}^{\text{air}}} \right| \tag{10.5}$$

Figure 10.5d illustrates the threshold voltage sensitivity ($S_{V_{\text{th}}}$). As seen, SVth enhanced with different BCC biomolecules. This improvement is attributed to the increased coupling capacitance within the nano-gap cavities, which enhances the device's performance. The highest $S_{V_{\text{th}}}$ is achieved with the MS-ES-TFET biosensor at $k=32$, indicating that the device performs optimally in detecting biomolecules with a higher dielectric constant, improving its effectiveness for cancer cell detection.

In Figure 10.6a, the I_{ds} sensitivity with varying NC biomolecule densities is evaluated using Equation (10.1). For increasing NC density proposed device's $S_{I_{ds}}$ improves due to enhanced transfer characteristics. The highest response is observed at a charge density of $-1\times10^{10}/\text{cm}^2$, specifically for MCF-10A (healthy) biomolecules. Figure 10.6b presents the graph of threshold voltage sensitivity ($S_{V_{\text{th}}}$) versus

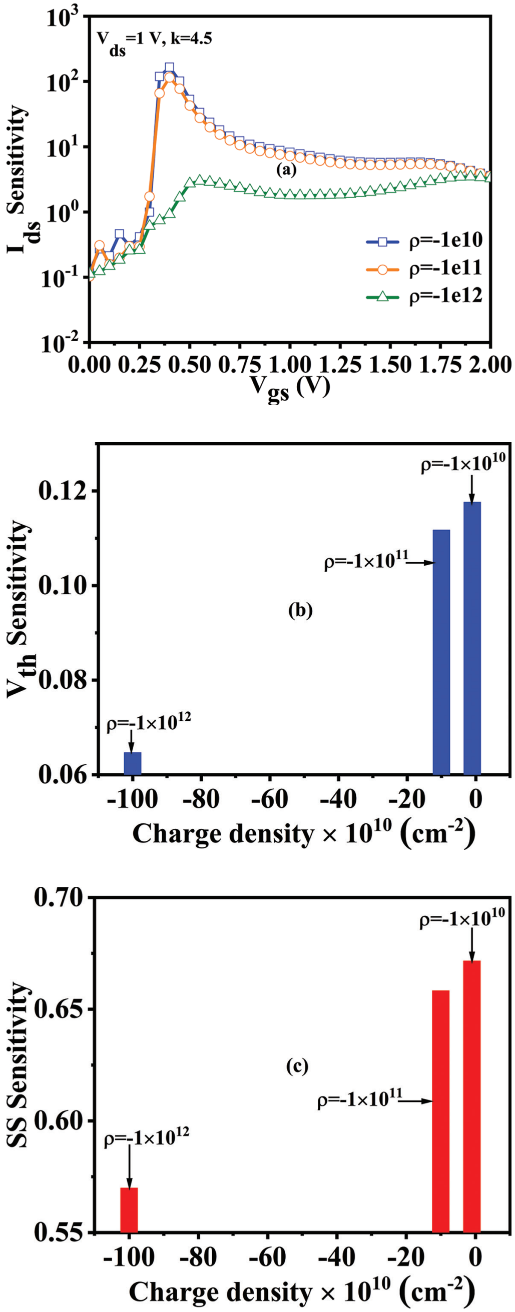

FIGURE 10.6 The negative-charged BCC biomolecules behavior in terms of (a) I_{ds}, (b) V_{th}, and (c) SS sensitivities at $V_{gs} = 2\,V$ and $V_{ds} = 1\,V$.

NC values, showing that $S_{V_{\text{th}}}$ increases with higher charged densities. The maximum value of 0.117 is achieved at $-1 \times 10^{10}/\text{cm}^2$ and $k = 4.5$. Additionally, the SS sensitivity is also increasing with rising NC density. This overall enhancement in sensitivity can be attributed to the stronger interaction between the charged biomolecules and the device's active region. As a result, the proposed device exhibits improved detection capabilities. From these graphs, it is evident that BCC molecules are detected more quickly and accurately at a charged density of $-1 \times 10^{10}/\text{cm}^2$, making it a promising tool for biomolecule sensing.

10.3.3 RF ANALYSIS

This section focuses on the analysis of RF parameters to offer insights into the high-frequency performance of the MS-ES-TFET biosensor. These parameter's analysis is essential for enhancing the device's performance in real-world applications, particularly in communication systems and biomedical sensors. By optimizing the RF characteristics, the biosensor can achieve better signal integrity and operational efficiency across a wide range of frequencies. Figure 10.7a illustrates the small signal gate-to-drain capacitance (C_{gd}) behavior along gate voltage under various BCC molecules. The C_{gd} rises with gate voltage because of the influence of the Miller capacitance effect [44]. Additionally, the C_{gd} increases as the dielectric properties of BCC molecules improve. In contrast Figure 10.7b illustrates that the gate-to-source capacitance (C_{gs}) decreases with increasing gate voltage (V_{gs}) due to the relatively constant electron concentration at the source side of the proposed device [44]. Furthermore, C_{gs} decreases with the increasing dielectric values of BCC molecules at $V_{\text{ds}} = 1$ V.

The cut-off frequency (f_T) is the point where a device starts to lose its effectiveness. It is formulated as $g_m/2\pi(C_{\text{gd}} + C_{\text{gs}})$. A higher transconductance results in a higher cut-off frequency, which indicates reduced parasitic capacitance in the proposed device [44–46]. Figure 10.7c illustrates the f_T response for different BCC molecules, showing that the device's cut-off frequency increases in the presence of cancer cells. The highest f_T is achieved with the $k = 32$ biomarker. Furthermore, the graph illustrating the transit time (τ) of the MS-ES-TFET device is shown in Figure 10.7d. It is calculated using the formula $\tau = 1/2\pi f_T$ [35]. The transit time reduces with improving permittivity of BCC molecules, indicating faster operation. For effective BCC detection, a lower τ is crucial, as it reflects quicker response times. The device achieves the fastest detection with the $k = 32$ biomolecules, making it more efficient compared to other BCC molecules in identifying BCC.

The device efficiency (DE) of the proposed MS-ES-TFET biosensor reflects its performance effectiveness. The DE is evaluated by: $\text{DE} = g_m/I_{\text{ds}}$, where g_m is the transconductance and I_{ds} is the drain current. Figure 10.7e illustrates the DE plot of MS-ES-HJ-TFET biosensor with gate voltage. The DE gradually enhanced for increasing neutral dielectric of the BCC molecules, reaching its peak at $k = 32$, with a maximum value of 25,000 V^{-1}. This indicates that the device becomes more efficient in operation as the biomolecule's dielectric constant rises.

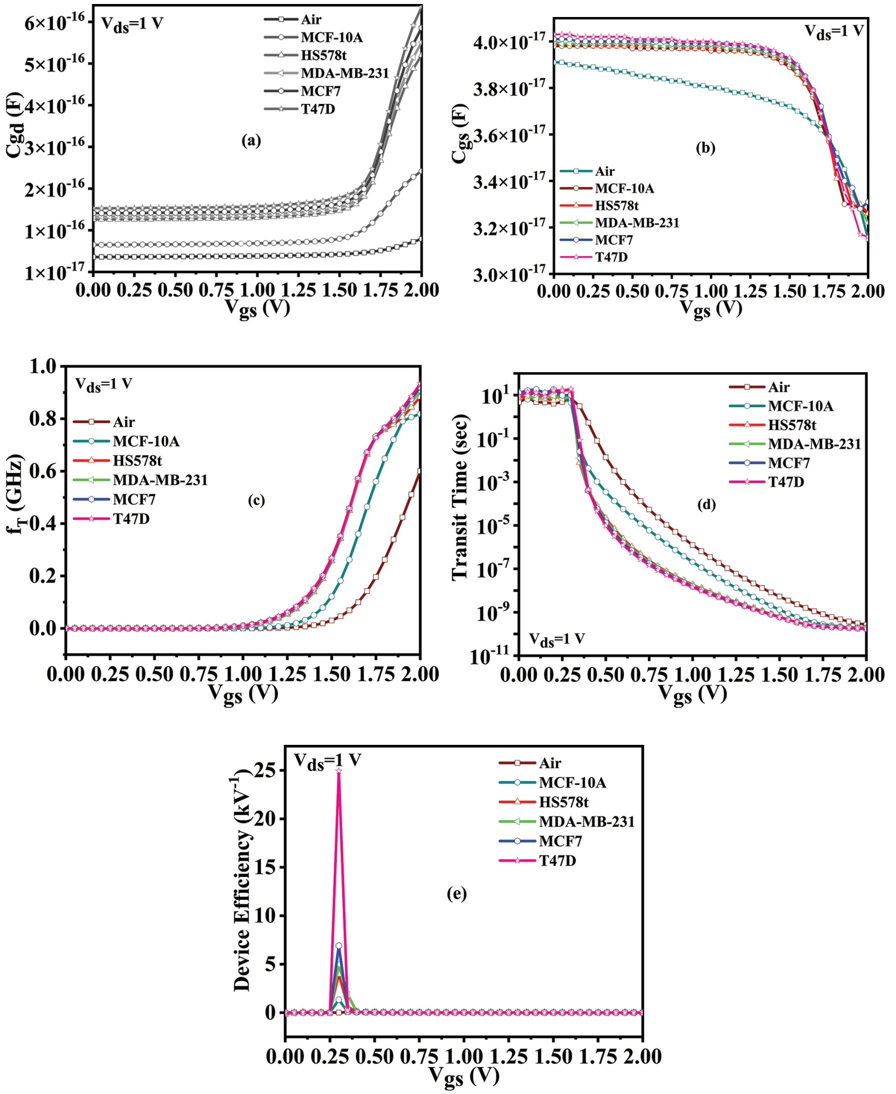

FIGURE 10.7 The plots of (a) C_{gd}, (b) C_{gs}, (c) f_T, (d) transit time (τ), and (e) device efficiency of the MS-ES-TFET biosensor device with variation of BCC molecules.

10.4 NONUNIFORM CONJUGATION EFFECT

The behavior of a nonuniform nano-gap cavity is analyzed with varying fill factors or density ratio (FF) of 25%, 50%, 75%, and 100%, and shown in Figure 10.8a–d. As the fill factor increases, the device's electrical properties enhanced. At a 25% fill factor, a significant portion of the nano-gap remains empty, leading to reduced interaction between the cancer cells and the cavity. As the fill factor reaches 50%, the

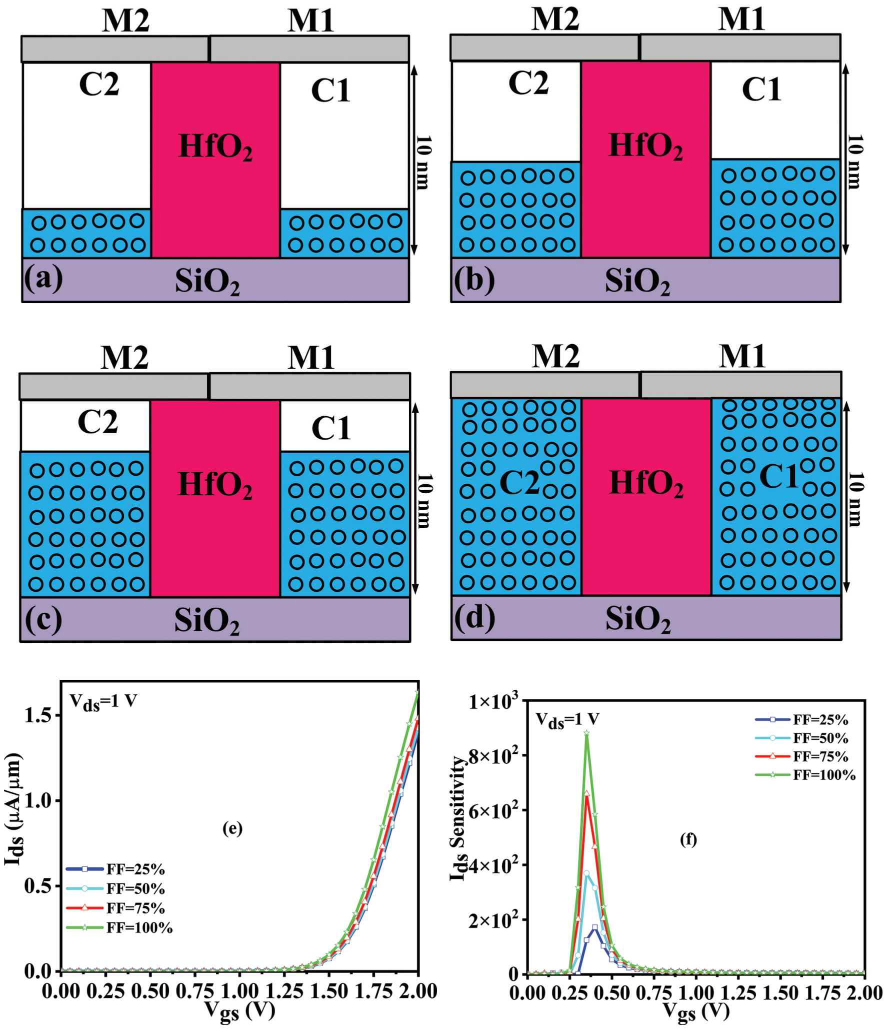

FIGURE 10.8 The nano-gap cavities with different fill factor: (a) 25%, (b) 50%, (c) 75%, and (d) 100%. Their respective (e) transfer characteristics and (f) I_{ds} sensitivity at $k = 4.5$ and $V_{ds} = 1$ V.

interaction strengthens, enhancing the cavity's performance in terms of energy transfer and signal transmission. With a 75% fill factor, the majority of the nano-gap is filled, resulting in improved confinement of light or charge carriers, further optimizing device efficiency. At 100% fill, the nano-gap is completely occupied, maximizing the interaction and ensuring the strongest possible coupling effect [34].

The impact of different fill factors on the transfer characteristics is illustrated in Figure 10.8e for the MCF-10A biomarker at $V_{ds} = 1$ V. As the density ratio increases from 25% to 100%, the I_{ds} of the proposed device shows little improvement.

This improvement occurs because a 100% fill factor provides maximum immobilization within the nano-gap cavities, leading to enhanced interaction between the biomolecules and the device's active region. The highest I_{ds} value, 1.05×10^{-6} A, is achieved at 100% FF, signifying optimal device performance. The increased fill factor ensures a more uniform charge distribution, improving the device's conductivity and response time [47,48].

The I_{ds} sensitivity, calculated using Equation (10.1), is shown in Figure 10.8f. The plot reveals that the sensitivity increases with a higher fill factor due to improved carrier mobility and stronger coupling between the biomolecules and the sensing surface [49,50]. The peak S_{Ids} reaches a value of 9×10^2 at $k = 4.5$, reflecting the enhanced sensitivity and detection capabilities of the device as the nano-gap cavities are fully occupied. This demonstrates that achieving a higher fill factor not only improves current flow but also significantly boosts the device's sensitivity to target biomarkers, making it more effective for precise detection applications.

10.5 CONCLUSION

The development of a dual-metal double-gate metal strip-loaded extended source-tunnel field-effect transistor (MS-ES-TFET) biosensor marks a significant advancement in breast cancer detection technology. The incorporation of novel features, such as the metal strip and extended source, enhances the tunneling rate and enlarges the tunneling area, improving overall performance. The biosensor detects BCC molecules by etching portions of the HfO_2 oxide layer beneath the gate metal through nano-cavities (C1, C2, C3, and C4). Detailed simulations and analyses investigate the dielectric properties of breast cancer molecules and their influence on electron and hole concentration, energy band structure, and electron tunneling rate. An enhanced response is observed at a dielectric constant (k) value of 32. The introduction of the metal strip and the extended source has resulted in significant improvements. The DC analysis of the proposed device considers important biomarker characteristics, including dielectric constant and charge densities. The T47D cancer cells exhibit a significantly faster detection rate compared to other healthy and cancerous cells. At a charge density of $-1 \times 10^{10}/\text{cm}^2$, the device demonstrates an improved response to negative-charged molecules. The sensing performance of the proposed device MS-ES-TFET is optimized at $k = 32$, demonstrating improved outcomes in terms of I_{ds}, g_m, V_{th}, SS, and I_{ratio}. In addition, radio frequency (RF) parameters, such as capacitance between the C_{gd}, capacitance between the C_{gs}, and f_T, τ, and overall DE are analyzed highlighting the device's potential for BCC diagnostics. Further, nonuniform conjugation effects characterized by different filling factors are investigated. It demonstrates the biosensor's adaptability and effectiveness in achieving optimal sensitivity. The improved immobilization mechanism for biomolecules enhances the device's sensitivity and accuracy in differentiating between healthy and cancerous breast cells. The study reveals a strong correlation between the dielectric properties and charge densities of BCC biomarkers and the electrical responses of the biosensor. Overall, the MS-ES-TFET biosensor offers a promising solution for an efficient breast cancer diagnosis and establishes a foundation for future advancements in biosensing technology, potentially improving patient outcomes through timely and accurate disease detection.

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11 Exploring Tunnel Field Effect Transistors (TFETs) as Label-Free Biosensors

Bridging Advances in Biosensing Technology

Basudha Dewan and Kamal Kishor Choure

11.1 INTRODUCTION

Since 1947, when the transistor was invented by William Shockleey, John Barden, and Walter Bratain at Bell Labs [1], and the subsequent creation of the Integrated-Circuit by Jack Kilby in 1958 [2], the repercussion about the unraveling of technology on the lives is immense. Today, it's unimaginable to live without it, considering the wide array of smart devices such as cars, phones, watches, TVs, and healthcare gadgets that simplify our daily routines. This transformation is primarily attributed to the continuous miniaturization of electronic transistors. The semiconductor industry has been driven by Moore's law, which outlines an explosive rise for the number of transistors on a single semiconductor chip [3]. Shrinking technology nodes and, consequently, reducing transistor channel lengths have enabled additional devices packed on top of an individual chip, leading to lower production costs and increased complexity. Additionally, the reduction in transistor size has facilitated the construction of quicker circuits with fewer watts of energy utilization per transistor. Till 1990s, semiconductor industry largely adhered to Dennard's transistor scaling theory proposed in 1974 [4]. This theory involved a proportional reduction in both V_{DD} and V_{TH} of transistors as channel length and width dimensions decreased. Consequently, as V_{DD} decreased, there was a quadratic depletion in the usage of dynamic power within the transistors therefore, consequently, in integrated circuits (ICs). The efficient scaling down of transistors is primarily attributed to exceptional physical and electric properties of SiO_2, which was utilized as the barrier layer between the device's gate and channel.

Over the last 15 years, various changes to the device structures have been necessary to sustain the trend of technology scaling. For instance, for 90 nm semiconductor node, strained silicon technology was established to improve carrier movement within transistors. This was achieved by employing techniques like incorporating SiGe semiconductors within the source/drain sections for P-channel metal-oxide-semiconductor transistors and utilizing a stretchable Si_3N_4-capped barrier for

DOI: 10.1201/9781003543923-11

N-channel metal-oxide-semiconductor transistors [5]. As gate oxide thickness decreased, one major challenge at the 45 nm technology nodes was a rise in gate loss caused by electrons passing across the narrow gate dielectric via tunneling. This issue is effectively addressed by introducing gate dielectrics with a higher dielectric constant ($\varepsilon_r = 25$ for HfO_2 compared to $\varepsilon = 3.9$ for SiO_2), considerably reducing gate leaking and enabling scaling up to 32 nm [6].

Following additional reductions in the length of the channel, there was a rise in the thermal diffusion of carriers and, consequently, an uptick in leakage current. This necessitated modifications to the traditional complementary metal-oxide-semiconductor (CMOS) construction. In order to counteract resulting rise in constant energy usage within chips, alternative semiconductor topologies like Fully Depleted-Silicon-on-Insulator (FD-SOI) and FinFETs have been created and already in fabrication, even reaching technologies that are as small as 7 nm [7].

FinFETs are classified under multi-gate technologies because they differ from conventional one-gate MOSFETs in that they include a gate electrode which surrounds the electrically conducting channel on multiple sides. Semiconductor devices featuring this manifold-gate layout enhance the gate's dominance over channel, facilitating mitigation of short-channel effects and subsequently reducing internal device leakage power [8].

As depicted in Figure 11.1, over the coming time, semiconductor devices are anticipated to shrink to just some nanometers, beyond this point, additional reduction in dimensions of transistors would become unfeasible [10]. As MOSFET dimensions approach a scale where they consist of only a few hundred atoms, unwanted phenomena like gate tunnel would impede future enhancements in efficiency because of significant

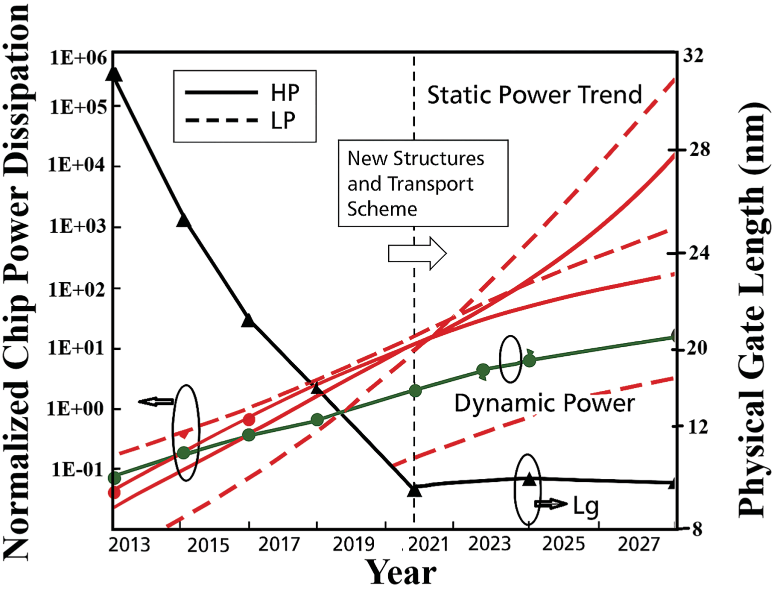


FIGURE 11.1 Trends in static and dynamic power dissipation concerning gate length in relation to technology, as sourced from ITRS 2015 [9].

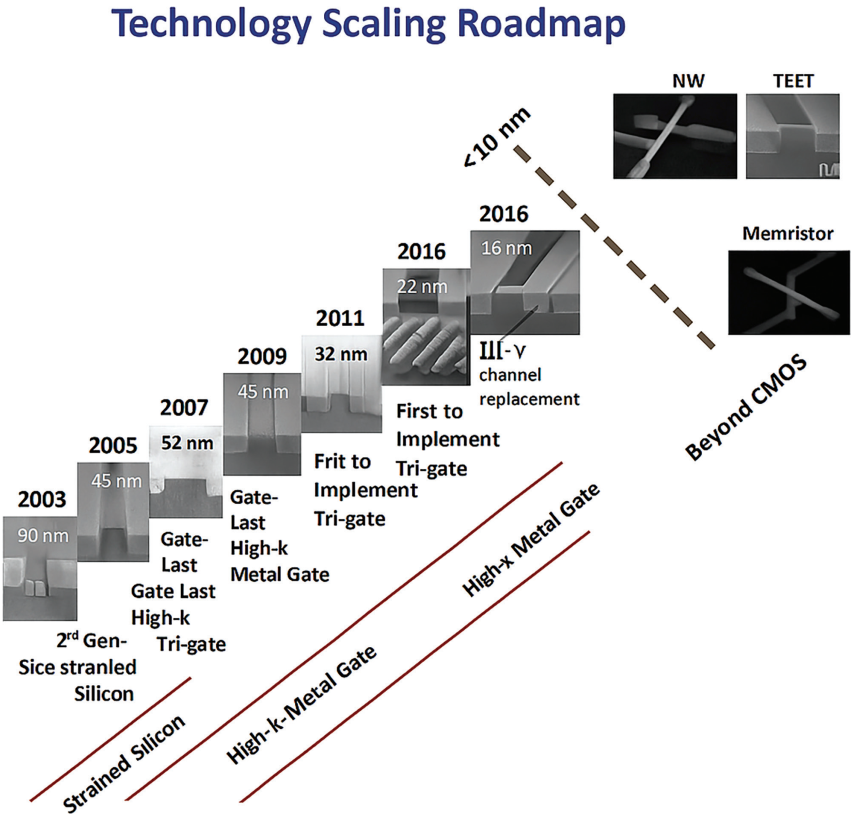

Technology Scaling Roadmap
NW
TEET
<10 nm
Memristor
2016
16 nm
2016
22 nm
2011
32 nm
2009
45 nm
2007
52 nm
2005
45 nm
2003
90 nm
III-V
channel
replacement
First to
Implement
Tri-gate
Frit to
Implement
Tri-gate
Gate-
Last
High-k
Metal Gate
Gate-
Last
Gate Last
High-k
Tri-gate
2rd Gen-
Sice stranled
Silicon
Beyond CMOS
High-x Metal Gate
High-k-Metal Gate
Strained Silicon

FIGURE 11.2 The roadmap for technology scaling: the past, present, and future [11].

leakage currents. In order to prevent subsequent rise in static power consumption as technology continues to shrink and to maintain the growth of transistor count with economically practical manufacturing methods, the industry of semiconductors would focus its attempts on developing vertical in nature instrument designs, circuits using numerous layers (three-dimensional integration), as well as alternative electric transfer approaches. This will necessitate creation of electronic devices using other elements, including Silicon-Germanium, Germanium, and other. In summary, Figure 11.2 illustrates the CMOS technology scaling roadmap to date, alongside emerging devices currently under research to achieve further transistor miniaturization [9].

11.2 NEW APPROACHES FOR UPCOMING TECHNOLOGY GENERATIONS

In order to mitigate the increasing tendency of static energy use in circuits at next-generation technical nodes, channel materials and structures must be modified. Following technologies are considered the most viable options to continue scaling technology down to dimensions in the nanometer range:

1. The 2015 ITRS roadmap forecasts that the next step in scaling MOSFET technology will involve replacing the stretched silicon path with superior movement materials. However, the shift presents several challenges that need to be addressed. These challenges include improving the interface between large-K dielectrics and Ge-III-V materials, minimizing band-to-band tunneling (BTBT) in narrow bandgap channel materials, and developing a manufacturable process for very-large-scale integration (VLSI) on a silicon platform. These are just a few of the many obstacles that must be overcome in this transition [11,12].
2. Nanowires (NWs) offer a promising avenue for replacing traditional planar MOSFET channels, potentially enabling a further reduction in technology node size. This is achievable because NWs can be manufactured with diameters in the nanometer range [13]. NWs are particularly well-suited for gate-all-around structures, which have the potential to mitigate short-channel effects. Their vertical growth orientation aligns with the future trend of vertically integrating devices on semiconductor chips. To ensure the growth of defect-free nanowires, there is a need to enhance both device yield and uniformity. Additionally, in case the transfer of NWs onto another medium becomes necessary, precise positioning becomes crucial. To avoid surface irregularities and defects, it is essential to develop effective surface treatment and passivation techniques.
3. Carbon Nanotubes (CNTs) are considered a promising choice for technology nodes below 10 nm due to their extremely thin bodies, approximately 1 nm in diameter. When compared to silicon, CNT-FETs can provide enhanced channel's electron as well as hole mobility, particular while at room temperature. However, challenges exist in terms of achieving VLSI integration with CNTs, including the need to purify and sort CNTs to ensure a relatively uniform diameter distribution [14].
4. Graphene Field Effect Transistors (GFETs) hold significant potential for the radio frequency (RF) design field due to their superior carrier mobility compared to CNTs. They enable the development of faster transistors with smaller dimensions. Graphene, being a solitary atomic sheet, essentially a no bandgap semiconductor. Consequently, the primary focus of research in this area is on finding ways to introduce a bandgap effectively. This is crucial for achieving a substantial current gain (I_{ON}/I_{OFF}) suitable for both analog and RF applications [15].
5. Tunnel Field Effect Transistors (TFETs) are highly regarded as the most promising technology for applications requiring low power and modest performance due to their unique electrical properties [16]. Unlike conventional thermal devices, TFETs utilize a distinct carrier injection mechanism, enabling them to maintain a reverse just below the threshold slopes (SS) of less than 60 mV/decade during ambient temperature. Because of this feature, TFETs may function at minimal voltages and yet have a substantial current amplification. Successful inclusion of TFETs into lower-energy circuits in the future hinges the advancement of III-V production methods. TFETs developed from materials from groups III and *V* show promise in surpassing the electrical performance of Si-based TFETs [17].

11.3 TUNNEL FIELD EFFECT TRANSISTORS (TUNNEL FETs) AS A VITAL TECHNOLOGY FOR ENERGY HARVESTING

One strategy aimed at cutting down on the amount of power consumed in digitally processed units is by lowering the electric source supply (VDD) for the electronic circuits. When VDD is reduced linearly, it results in a quadratic decrease in dynamic power consumption. Having said that, provided the transistor's threshold voltage (VTH) fails to increase proportionately to VDD, the fails to increase proportionately to VDD, the current loss increases exponentially, leading to higher static power consumption. This issue is tied with the thermally controlled charge infusion process in traditional MOSFETs. The reverse beneath the threshold slopes (SS) cannot be more than 60 mV/dec. As a result, lowering VDD causes a sharp rise in beneath the threshold current loss, as illustrated by Equation (11.1) [18,19].

$$I_{\text{sub}} = K_1 W e^{\frac{-V_{\text{TH}}}{\eta V_\theta}} \tag{11.1}$$

Beneath the threshold current loss formula includes constants K_1 and n, which are determined through experimental measurements. It also involves the transistor's width (W) and the thermal voltage (represented by V_t, which is approximately 25 mV at room temperature). According to Figure 11.4, threshold values of voltage in transistors in exceptionally well along with subpar performance utilities are projected to remain incessant in the coming times.

As the power supply voltage (VDD) decreases, there will be an anticipated increase in leakage power within integrated circuits, as illustrated in the power trends displayed in Figure 11.1. However, the introduction of various technologies that incorporate new materials and transport methods, which are not reliant on thermal effects, will enable a reduction in the threshold voltage of transistors without causing a corresponding increase in static or standby power consumption in chips.

As of now significant exploration is focused on developing switches having exceptionally sharp sub-threshold dynamics, specifically below 60 mV/dec at room temperature. Among various alternatives employing different carrier injection mechanisms, the TFET is emerging as the most promising technology for switches designed to operate at low voltages (below 0.5 V) and in applications with lower performance requirements [20,21].

As shown in Figure 11.5, the TFET device provides the benefit of lowering the overdrive voltage (VGS − VTH) while still achieving better functionality from the perspective of reducing off-state current along with minimizing static energy utilization when contrasted with mainstream temperature-based MOSFETs. Given its superior execution at reduced voltages, the TFET is well-suited for super subdued power, minimal functionality circuit boards, such as those used in internet of things sensor nodes, which rely on ambient energy sources for power (Figure 11.3).

11.4 TUNNEL FET TECHNOLOGY: STATE OF THE ART

In 1958, a researcher from Japan named L. Esaki, working at Sony Corporation, made a pivotal breakthrough by introducing a device that operated upon BTBT, designated as the tunnel diode. This device's working principle, grounded in quantum

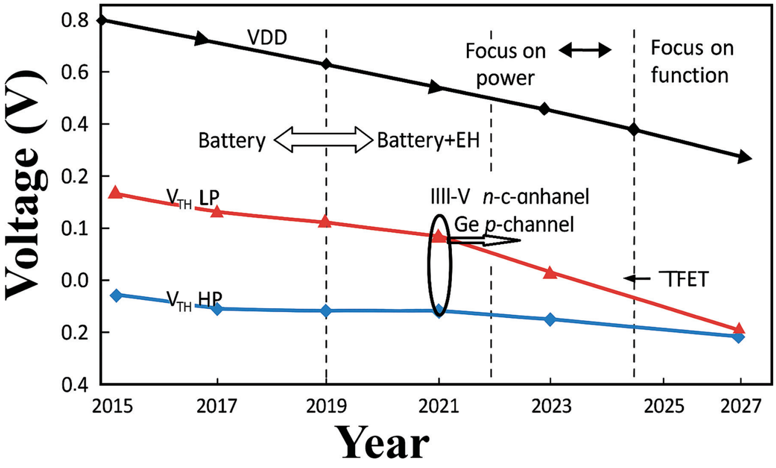


FIGURE 11.3 The voltage evolution observed in logic technology, as sourced from the ITRS 2015 report [9].

mechanics, differed significantly from transistors and further semiconductor devices of that era. In tunnel diodes, electrons could seemingly disappear from one side of a potential barrier and reappear on the other side without having enough energy to cross over the barrier directly [22]. This phenomenon, known as tunneling, allowed electrons to pass through the depletion region in p-n junctions.

Initially, the importance of the tunnel diode wasn't fully realized, primarily due to limited knowledge about the tunneling process. However, decades of research have highlighted tunneling as a promising solution for emerging switching technologies, particularly because of its ability to function effectively at low voltages, typically below 0.5 V.

Esaki, while studying internal field emission in semiconductor diodes with heavily doped germanium (Ge) junctions, observed a nonlinear current–voltage relationship when subjected to forward bias at low temperatures. This phenomenon, linked to the elastic nature of tunneling in Ge, resulted in the identification of negative differential resistance (NDR). Importantly, the tunneling process maintained the electron's energy during the transition.

Esaki's work had far-reaching implications, earning him the Nobel Prize in Physics in 1973. His discovery profoundly influenced several fields, including radio transmission, amplification, computation, and DC-AC conversion, all benefiting from the NDR effect observed in tunnel diodes (Figure 11.4).

11.5 BAND-TO-BAND TUNNELING (BTBT) CURRENT

In classical mechanics, particles are constrained by potential barriers, and only those possessing energy exceeding the barrier's height can transition from one region to another through thermionic emission. In contrast, quantum mechanics describes particles using wave functions denoted as Ψ, which do not abruptly cease at finite potential barriers of height U_0. Consequently, there exists a finite probability of particles

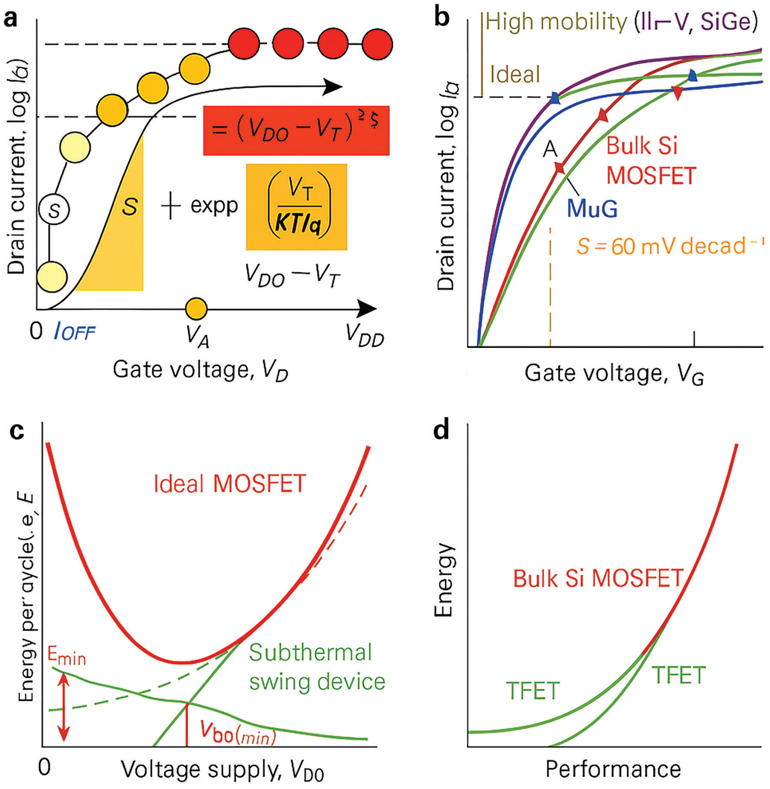


FIGURE 11.4 Characteristics pertaining to input behavior for MOSFETs and Tunnel FETs.

tunneling through the barrier and moving from one region to another [23]. In a tunneling device, we can distinguish between two categories of tunneling current: Zener tunneling current, which involves electrons moving from the valence band to the conduction band, and Esaki tunneling current, which entails electrons transitioning from the conduction band to the valence band (Figure 11.5).

In a tunneling device, the current is determined by the tunneling transmission probability, denoted as T_{BTBT}. The calculation of tunneling current involves applying the Wentzel–Kramers–Brillouin (WKB) approximation, which provides the tunneling transmission coefficient as defined in Equation (11.2) [24].

$$T_{\text{BTBT}} \cong \exp\left[-\frac{4\sqrt{2m^{*}}E_g^{1.5}}{3\hbar qF}\right] \tag{11.2}$$

11.6 REPORTED WORK

In this exponential rising scientific world, biosensors have become more considerable element in human life, which gave rise to a significant research area for the same. In this regard, the miniaturized CMOS compatibility dielectric modulated

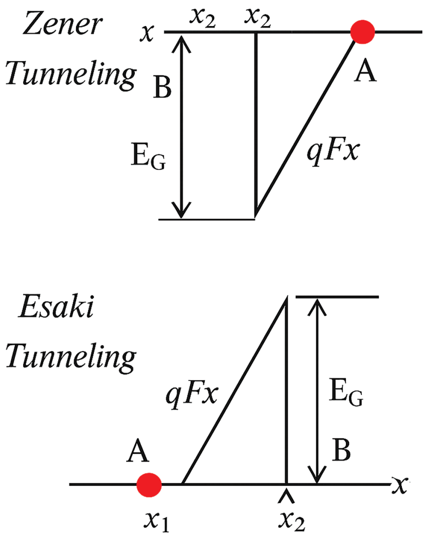


FIGURE 11.5 Potential barrier for (a) Zener tunneling and (b) Esaki tunneling.

FET (DM-FET) based biosensor shows satisfactory performance [25,26]. The dielectric modulation technique provides label-free detection of biomolecules through label-used detection challenges. A nanocavity is formed in DM-FET-based biosensor through removing a small percentage of the gate dielectric, where neutral/charged biomolecules can be occupied [27,28]. The DM-FET electrically detects the biomolecules based on dielectric constant and drain current by monitoring the targeted biomolecules confined to a cavity presented beneath the gate to immobilize the biomolecules [29]. The DM-FET-based biosensors suffer from scalability problems like higher leakage current, inability to reduce SS below 60 mV/dec. Due to these issues, DM-Tunnel FET (TFET) based biosensor is proposed, which can suppress the limitations of FET-based biosensor by several orders [30,31]. The enactment of TFET-based biosensors is enhanced due to BTBT rate at the source and channel interface [32], in addition to advantage of CMOS compatibility fabrication process and low leakage current. It can operate at very low power supply with significant reduction in power dissipation of the circuit. A biosensor of nanowire TFET architecture of positively charged is highlighted in literature [33]. The sensitivity of a dopingless DG TFET biosensor is highlighted for a wide changes in cavity height [34]. It is seen that short-gate TFET-based biosensor has improved sensitivity compared to full gate TFET biosensor [35]. An analytical model for sensitivity is revealed in DG TFET with the variant in *k* [36]. It is reported that circular gate (CG) TFET has more sensitivity than Ge source TFET at diverse *k* under neutral/charged biomolecules [37]. The vertical TFET has greater amount of sensitivity compared to DG TFET for uncharged/charged biomolecules at different values of *k* [38]. We have reported that Ge source DG TFET has better sensitivity compared to DG TFET for both neutral/charged biomolecules [39]. A DG TFET is widely used as it provides better control over the channel due to the presence of two gates and sensitivity is improved compared to a single gate [40]. Furthermore, to enhance the performance like SS and drive current, a structure known as ESDG-DM-TFET based biosensor is proposed [41]. It provides a comparatively improvement in current sensitivity and SS due to its enhanced tunneling junction area. The central focus of this paper is to evaluate the sensitivity of ESDG-DMTFET based biosensor under neutral/charged biomolecules for a wide variation in *k*. The SS and ION/IOFF ratio is reported at different k in ESDG-DMTFET. The sensitivity is extracted by considering steric hindrance in ESDG-DM-TFET at two different fill factors (45% and 65%). Moreover, the sensitivity of the proposed biosensor is compared with existing biosensor in literature.

11.7 DEVICE ARCHITECTURE AND SIMULATION DECK

The 2-D cross-sectional view of the proposed nanogap embedded extended source DG (ESDG) dielectric modulated TFET biosensor is shown in Figure 11.1. The corresponding symbol represents the various dimensions of the structure. The ESDG-DMTFET is a symmetrical dual gate structure, where source, channel, and drain are made of silicon. The doping concentration for *p*+ source, *n* channel, and *n*+ drain regions are 5×10^{18}, 1×10^{15}, and $10^{20}/cm^3$, respectively. The source region is prolonged into an n channel so that the channel overlaps the source. The gate material consists of single metal having work function of 4.05 eV. The nanogap is created on both sides of source/drain regions by removing out HfO_2 and the existence of these nanogap growths the capture area of the biomolecules. A thin SiO_2 layer of 1 nm thickness is taken as an immobilizing layer for biomolecules present in the nanogap. The various dimensions of the proposed biosensor are listed in Table 11.1 (Figure 11.6).

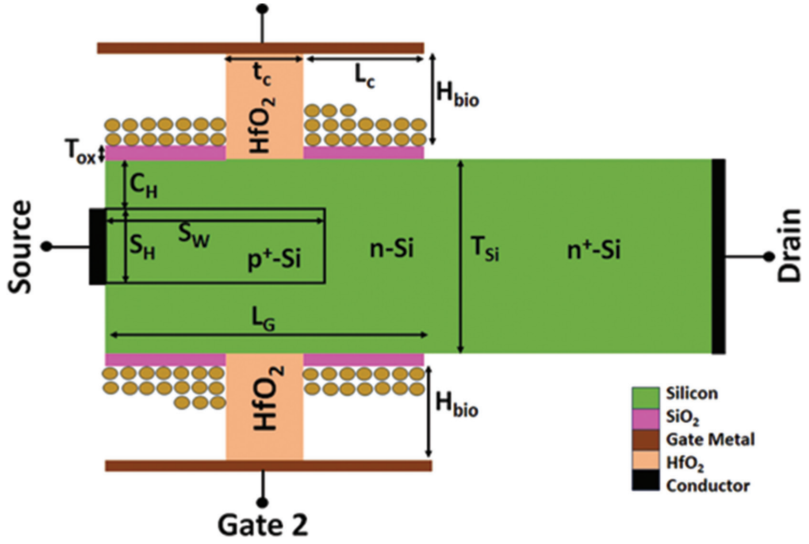


FIGURE 11.6 2D view of nanogap ESDG-TFET biosensor.

TABLE 11.1
Dimensions of the Proposed Biosensor Considered in this Work

Parameters	Value (nm)
Silicon film thickness (T_{SI})	15
Source height (S_H)	10
Source length (S_W)	20
Channel height (C_H)	2.5
Gate length (L_G)	30
The thickness of the SiO_2 layer (T_{OX})	1
Length of nanogap cavity (L_C)	12.5
The thickness of the HfO_2 layer (t_h)	5
Height of nanogap cavity (H_{bio})	7

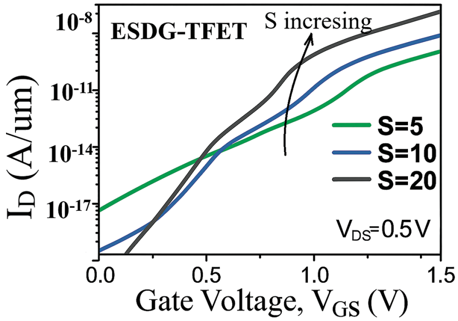


FIGURE 11.7 Transfer characteristic of ESDG-TFET at different source length.

Technology computer-aided design (TCAD) simulator is employed to extract the sensitivities of the ESDG-DMTFET [42]. The probability of tunneling in TFET be determined by the energy bandgap and accordingly, bandgap narrowing is used. The degenerate source and drain sections leads to activation of Fermi distribution model. For accurate simulation, Shockley-Read-Hall (SRH) is also adopted for recombination process in the simulator. The non-local BTBT model is activated to analyze the transport of the charge carriers. The experimentally calibrated tunneling parameters are invoked in simulator: $A_{path} = 1.63 \times 1014\,cm^3/s^1$, $B_{path} = 1.47 \times 107$ V/cm, $P_{path1} = 0.0567\,eV$ [43]. During simulation, a low range of k (2–5) and high k value (5–12) biomolecules are considered in the cavity. The example of uncharged biomolecules are uricase = 1.54, protein = 2.5, streptavidin = 2.1, APTES = 3.57, etc. The positive and negative charge concentrations are considered as mentioned in literature for DNA [44–46].

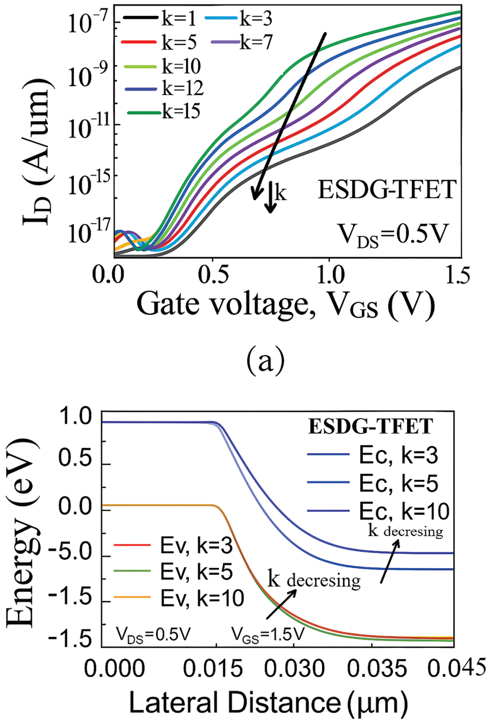
The transfer characteristic of ESDG-TFET at different source length is shown in Figure 11.2. It is realized that the increased in source length improves the switching ratio and this is due to increase in tunneling area which leads to increased BTBT rate at tunnel junction (Figure 11.7).

11.8 RESULTS AND DISCUSSION

Here, the characteristics of ESDG-DM-TFET biosensor is analyzed for $k=5$, 7, 10, 12, and 15. The neutral and charged biomolecules are undertaken to measure the sensitivity of this biosensor at stated k. The output of this biosensor is dignified considering the effect of steric hindrance. Here, $k=1$ implies the nanogap is filled with air.

11.9 SENSITIVITY ANALYSIS FOR NEUTRAL BIOMOLECULES

The input drain current characteristic of ESDG-DMTFET at various k for neutral charged molecules ($N_{\text{bio}}=0$) is shown in Figure 11.3a. The rise in k leads to significant enhancement in ON current and this is due to rise in tunneling rate at the tunnel junction. It can be better clarified from Figure 11.3b, where the energy band diagram is plotted as a function of k and it is envisioned that the increased in k, lessens the tunnel width for ESDG-DMTFET. This leads to increase in number of charge of carriers and thus, ION is increased. The performance of biosensor can be extracted from its sensitivity and for DM-FET, the sensitivity mathematically is defined as [47] (Figure 11.8):



(a)

(b)

FIGURE 11.8 Input characteristic of (a) ESDG-DM TFET biosensor and (b) corresponding energy bandgap for uncharged biomolecules with variation in k.

$$\text{Sensitivity, } S_n = \frac{I_{D,k}}{I_{D,\text{air}}} \tag{11.3}$$

where $I_{D,k}$ and $I_{D,\text{air}}$ are represents the corresponding drain currents for $k > 1$ and $k = 1$, respectively, at fixed gate voltage (V_G) and drain to source bias (V_{DS}).

The sensitivity for the variation in k for ESDG-DMTFET is portrayed in Figure 11.4a, and it is summarized that S_n is increased by an observable amount with k due to enhancement in I_{ON}. It is observed that sensitivity in range of 10^4 at $k = 15$ is achieved. The effect of k on SS and $I_{\text{ON}}/I_{\text{OFF}}$ ratio is shown in Figure 11.4b and SS is expressed as [47]:

$$\text{SS} = 2.3\eta V_T \tag{11.4}$$

where V_T and η are thermal voltage and sub-threshold slope, respectively. The η is given by

$$\eta = 1 + \frac{C_{\text{dep}}}{C_{\text{ox}}} \tag{11.5}$$

where C_{dep} and C_{ox} indicate the depletion and oxide capacitances, respectively. It is perceived from Figure 11.4b that the increase in k reduces the SS and this is due to decrease in η. It is also visualized that for all values of k, the SS value is below 60 mV/dec., which indicates ESDG-TFET can be used for low power applications. The rise in k leads to significant escalation in ON current with negligible changes in OFF current, which indicates improvement in $I_{\text{ON}}/I_{\text{OFF}}$ ratio for ESDG-DMTFET (Figure 11.4b).

11.10 CONCLUSION

This chapter delves into the intricate construction of ultra-low power circuits tailored specifically for energy harvesting through the utilization of TFETs. TFETs stand out due to their BTBT carrier injection mechanism, rooted in the Zener tunneling effect. This mechanism grants TFETs a sub-threshold slope (SS) that operates inversely to the typical limit of 60 mV/dec observed in conventional thermally dependent switching devices at room temperature. The remarkable characteristic of TFETs allows for the reduction of operational voltage in circuits without compromising the device's leakage current. Consequently, A DM Extended Source double-gate (ESDG)-TFET biosensor is designed and its Sn is reported. We have highlighted Sn underneath neutral and charged biomolecules with wide variation in k within the nanogap cavity and the upsurge in k leads to improvement in Sn. Therefore, ESDG-DMTFET biosensor is an emerging device for bio sensing applications due to its enhanced performance.

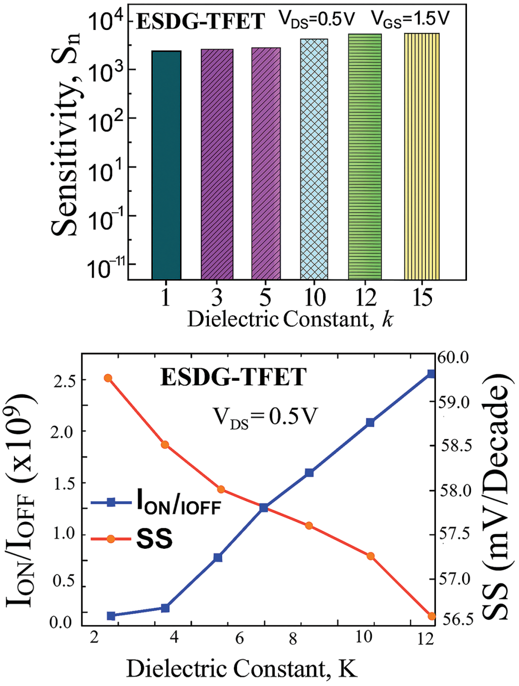


FIGURE 11.9 (a) Sensitivities of ESDG-DM TFET biosensors $k=5$, 7, 10, 12, 15 and (b) I_{ON}/I_{OFF} and SS at these k.

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12 Field Effect Transistors in Gas Sensing

Advances in Detection and Analysis of Diverse Gases

Ankit Kumar Singh, Sanjeev Rai, and Nirmal Roy

12.1 INTRODUCTION

The growing need for gas detection has resulted in the invention of more reliable gas sensors with enhanced sensitivity and faster response times. Different types of gas sensors including optical gas sensor, electrochemical gas sensor, and field effect transistor (FET)-based gas sensor are being developed to enhance the detection and analysis of target gases. Optical gas sensors function through the determination of gases by direct measurements of the gas properties such as absorption, emission, or refractive index, providing a fast response and high sensitivity. Such optical sensor usages also lead to a reduction in the physical sizes of the devices because of simplifying the construction. While their limitations come from the fact that they are oversized and are costlier than for instance electrochemical and FET sensors [1–4]. Electrochemical sensors detect electrochemical processes between the target gas and the sensing electrode, which provide an electrical signal proportional to gas concentration using oxidation or reduction reactions. These sensors are very sensitive and specific in nature and can detect gases at very low concentrations (sub-ppm level) through oxidation or reduction reactions. But these sensors can operate only within a very limited temperature range because there is a risk of the electrolyte getting dried at elevated temperatures or low humidity. Also, they may suffer from cross-sensitivity, whereas an adjustment in humidity affects the measurement of gas concentration [5–7]. As an alternative, FET gas sensors make use of the change of electric characteristic of the sensing material exposed to volatile organic vapors. They demonstrate advantages of high sensitivity, Quick response time, functioning at room temperature, and low power usage, and facileness in integration with electronic circuits. FET sensors are becoming a very good substitute for gas detection since they are highly sensitive and selective. Regarding all sensor types, the selection of sensing materials is one of the factors that narrow the performance parameters with respect to sensitivity, selectivity, repeatability and stability.

Changing the semiconductor channel's electrical characteristics is the basic idea underlying FET-based gas sensors. This happens through interactions between gas molecules and a sensitive layer on the FET's gate. When the target gas molecules

DOI: 10.1201/9781003543923-12

stick to this sensitive layer, they have the ability to change the charge carrier concentration. This might change mobility or threshold voltage of the FET. Consequently, we have an electrical signal that can be measured. FET-based gas sensors offer great potential in terms of modification for various types of gas. The effectiveness of detecting certain gases can be increased by the optimal selection of materials. These sensors have been examined in one form or another with different materials over the years. Among these are Metal Oxides Nanomaterials based on carbon Polymers with Conductivity organic semiconductors. It is essential to choose the sensing material properly. This results in changes to the sensor's sensitivity, selectivity, and reaction time [8–15].

The most investigated metal oxide-based FET gas sensors have low prices, quick reaction times, and excellent sensitivity. These sensors typically detect changes in electrical characteristics of a metal oxide layer on interaction with target gas molecules. It is possible to recognize metal oxides chosen for gas sensors based on their electrical structure. We may further enhance the performance of metal oxide-based FET gas sensors by doping or nano-structuring the gas sensor's sensing layer [16].

Now, we discuss carbon-based nanomaterials such as carbon nanotubes (CNTs) and graphene are popular choices for FET-based gas-sensing applications because these materials have large electrical gains and surface properties that make them very sensitive to changes in gas molecules which are interacted with the sensing layer. There is a wide range of CNT shapes, and as this busy field of study expands, more forms are being designed and manufactured. When we use carbon nanomaterials in FET-based gas sensors, they can exhibit excellent sensitivity, fast response, and good selectivity, especially when combined with additional features or heterojunction designs [17].

A conductive polymer (CP) such as polyaniline and polypyrrole that are also used in FET-based gas sensors. CP with larger surface areas and conductivity have improved sensor performance, increasing sensitivity, versatility and possibilities. These can be easy to design, flexible, and adaptable to specific gas detection needs. When these sensors operate, the charge transport in the polymer layer changes upon exposure to the target gas [18]. Advances in manufacturing technology may enable the incorporation of several levels of complexity into CPs based on the mixing and polymerization of various CP monomers, metallic particles, two-dimensional materials, carbon nanoparticle and copolymers. Now let us talk about organic semiconductor-based FET gas sensors. These are very useful for us because they are low cost, flexible and reliable for very large-scale production. It is crucial to choose the best organic semiconductor more carefully by considering how the electrical response of the sensor active material corresponds to its surface chemistry. These sensors use organic materials (graphite and carbon nanotube) or conjugated polymers (polyaniline and polypyrrole) as the semiconductor channel. With this approach, we can identify a variety of gas detection and analytes [19].

Apart from the selection of appropriate sensing materials, the design of a FET-based gas sensor is most importance factor, which determines the performance of gas sensor. Various architectures such as catalytic gate FETs, suspended-gate FETs, and nanomaterial-based FETs have been investigated [20].

12.2 VARIOUS STRUCTURES OF FET GAS SENSOR

The basic structure of the FETs is generally made by combining the gate electrodes, source terminal, drain terminals and a sensing layer. A gate voltage across the source terminal and the gate electrode can be employed to regulate the connection between the semiconductive material channel and conducting carriers across the drain electrode. By changing the electrical conductivity of the sensing material by contact with the target gas on the sensing area of the gas sensor, this enables for the identification and evaluation of various gases. Metal oxides or other sensing materials are typically used to create the sensor layer. Target gas interaction with this sensing layer affects the current flow between source and drain by altering the conductance of the channel and the surface potential. Gas concentrations are determined by observing changes in the current flowing between the source and drain terminals.

12.2.1 Top-Gate FET Gas Sensors

In general, the construction of the top-gate FET gas sensor is made up of an insulating layer, a top gate that is built using a catalytic metal or conductive oxide material, a more precisely defined semiconducting material (like graphene or a transition metal dichalcogenide) which is also connected to source and drain terminals. A typical structure is shown in Figure 12.1. When gas molecules deposit on the gate electrode of a top-gate FET gas sensor, the electrical characteristics of the semiconductor channel are progressively changed. To determine if how much the target gas is present and at what concentration, anyone can observe the change in the threshold voltage or channel conductance. Top-gate FET gas sensors provide many of advantages, including the possibility for reduction in size and integration into sensor sets as well as the ability to relate the sensing element with electrical circuitry [12]. Several materials and designs for top-gate FET gas sensors have been investigated over time by researchers. These materials and designs include metal oxides, polymers, and two-dimensional materials for the semiconductor channel or gate electrode. Numerous gas including hydrogen, carbon monoxide, volatile organic compounds, and hazardous industrial gases are being found to be sensitive to these sensors [20].

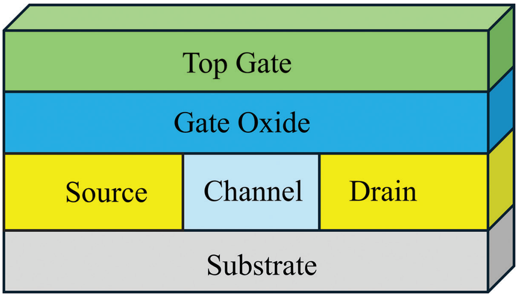


FIGURE 12.1 Top-gate FET gas sensor.

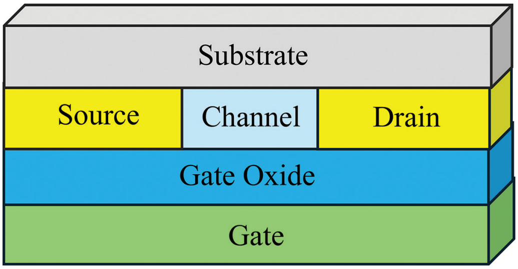


FIGURE 12.2 Back-gate FET gas sensor.

12.2.2 BACK-GATE FET GAS SENSOR

Back-gate FET gas sensors are most used gas sensor designs. This is made up of a semiconductive channel, a source terminal, a drain terminal, a back-gate terminal and a gate oxide layer. Figure 12.2 shows a typical example of this construction. The semiconductive material's electrical characteristics change as it comes into contact with gas molecules. This design allows it accessible to apply a bias voltage to the back gate, which can improve the performance of the sensor. Sensor restoration can be challenging by the complex modifications in semiconductor materials created by the direct interaction of gas molecules with the surfaces of the detecting channels. Furthermore, the absorption of non-target gas particles causes durability issues with this type of sensor design [21].

12.2.3 DUAL-GATE FET GAS SENSOR

The illustration of the dual-gate FET consists of semiconductive material channels, insulating oxide layers, a top and bottom gate, and a source and drain terminal, among other things. The above arrangement offers two layers of insulation in front of the semiconductive channel. The bottom gate creates significant increases by pushing the transistor to saturation, while the top gate manages its interactions that occurs between analytes.

In addition to being highly sensitive, the dual-gate structure of the sensor ensures excellent selectivity by improving its ability to distinguish between various gases. The poor condition of the connection between the semiconductor and the top dielectric layer usually reduces the performance. The efficiency of the sensor is restricted by this low interface quality, which prohibits the conduction channel from developing effectively at the top interface. Conventional dual-gate structures depend on variations in the bottom gate's threshold voltage carried on by charges on the top gate for detection. For real-time detection, however, this approach is not suitable. The selection of semiconductive materials becomes essential to obtaining around this limitation. Semiconducting polymers have been shown to be capable of offering smoother surfaces, which improves conduction directions along the top surface. To further enhance the overall performance of the sensor, the top gate must be functionalized, This indicates that it must be altered or handled in order to enhance its ability to interact with the target molecules [22,23] (Figure 12.3).

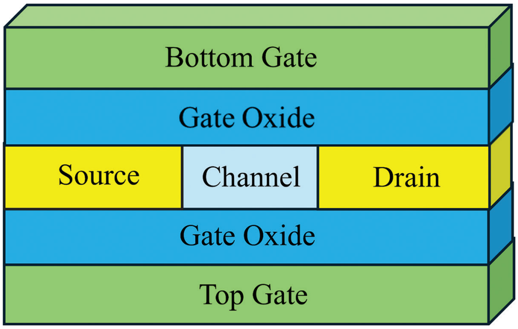


FIGURE 12.3 Dual-gate FET gas sensor.

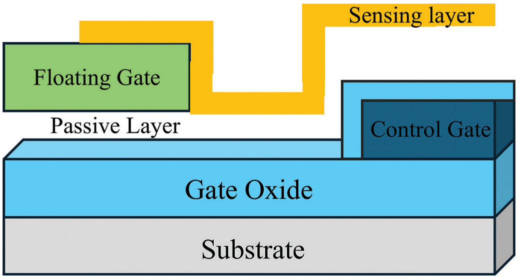


FIGURE 12.4 Floating-gate FET gas sensor.

12.2.4 Floating-Gate FET Gas Sensor

Gas-sensing technology has particularly popularized an advanced gas sensor known as the floating-gate FET gas sensor. An essential part of a floating-gate FET gas sensor is the floating gate, which is suspended by an insulating layer from the bulk as well as the source and drain terminals. In most instances, the floating gate that is made up of a conductive material such as polysilicon has a dielectric membrane that serves as a sensing element on it. The sensing material is designed in a manner that it has a large area of surface and strategic positions for the target gas to adsorb such that bonding actions are effectively transduced into electrical signals that can be read. When target gas molecules contact with the floating-gate sensing material, the material's work function, conductivity, or permittivity may change. The FET subsequently gathers these modifiers and changes the variations in physical characteristics into variation in the electrical characteristics of the device such a voltage or channel current [24] (Figure 12.4).

12.3 TYPES OF FET GAS SENSORS

FET gas sensors are an innovative family of chemical sensors that use the basic concepts of semiconductor technology to identify and analyze the presence of specific gases. These sensors are extremely sensitive and selective because they operate by taking benefit of the changes in a FET's electrical properties based on interaction with gas molecules. FET gas sensors are highly versatile due to their flexibility to be constructed in many ways, each specifically designed to detect various kinds of gases and chemical species. The different types of FET gas sensors are covered in the sections that follow along with details about their structures, common applications, and operating principles. Suspended-gate FET gas sensor (SGFETs), Catalytic metal-gate FETs gas sensor, Thin-film transistors (TFT), capacitively coupled FETs gas sensor (CCFETs) and horizontal floating-gate FETs gas sensor (HFGFETs) are a few examples of FET-type gas sensors [25].

12.3.1 Suspended-Gate Sensor

A suspended gas sensor can essentially be defined as a device that detects, recognizes, and quantifies gas molecules in its surrounding environment. Figure 12.5 presents the configuration of a basic suspended-gate FET gas sensor. To work these types of sensors, a sensing medium usually within the meaning of a semiconductor material, is either placed in air or between the two electrodes. There is a change in electrical characteristics of the suspended sensor when target gas molecules are present and the sensor is disturbed. This versatility comes from the fact that suspended gas sensors can be applied for outdoor or indoor industrial purposes. This is as a result of synergistic design where the sensor is placed such that the surrounding air is able to get in the sensor very fast and so within a fraction of a second the sensor can recognize and respond to changes in gas level. Central suspension skirt is another important component of a suspended gas sensor whereby the sensing material can either be a metal oxide or carbon-based material. In order to avoid disruption in the operation of the sensor, this support structure can be simplified to a lattice or an array of electrodes. The electrical properties of sensing materials, such as resistance or capacitance, change because of the interactions among target gas molecules with the suspended sensor.

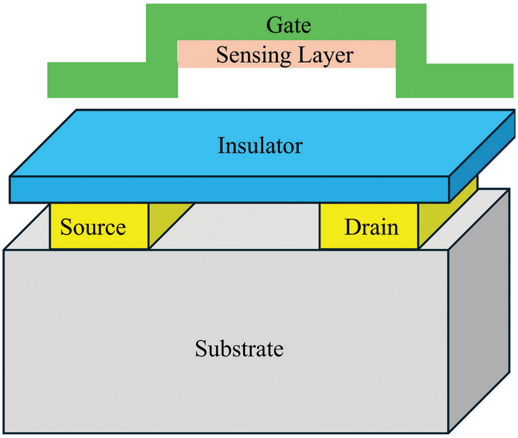


FIGURE 12.5 Suspended-gate FET gas sensor.

Hence, it is possible to evaluate the gas concentration by finding the resistivity and capacitance of the sensor material, and how the two changes over the period. Furthermore, the performance of the device may be enhanced via changing the structure, chemical nature of the sensing material, and the ambient parameters, such as temperature and humidity [26,27]. They are an advantageous instrument for many applications due to their great sensitivity and selectivity, as well as their capacity to function in a wide range of situations.

12.3.2 Catalytic Metal-Gate Sensor

The catalytic metal-gate FET sensor operates on a concept that target gas molecules change the work function of gate metal (such as palladium, platinum, or iridium). There are three physical and chemical processes that may be used to describe the sensing principal of the catalytic metal gas sensor for gas-sensing application. These are follows:

1. Surface reactions on the outer surface of the metal gate absorb gas molecules.
2. Dissociated gas molecules penetrate through a catalytic metal layer.
3. A dipole layer forms at the metal-gate insulator interface.

Gas molecules interact and separate on the catalytic gate surface, changing the charge distribution at the contact between gate and insulator. The fundamental construction is given in Figure 12.6. It in turn, modifies the drain-to-source voltage (V_{DS}) of the FET while retaining a constant current. The electrical performance of the sensor and the chemical processes that cause the gas response are defined by the selection of the catalytic metal and gate insulator materials. Catalyst metal gas sensor was first discovered by Lundstrom in 1975 and implement a catalyst gate which was formed by palladium metal. In comparison to other gas sensor types such as limiting-current and resistive sensors, catalytic metal-gate FET sensors do not require a current to flow through the sensing material rather than they amplify the gas-sensing signals, allowing for highly sensitive detection of target gases like nitrogen oxides, oxygen, and ammonia [12,28].

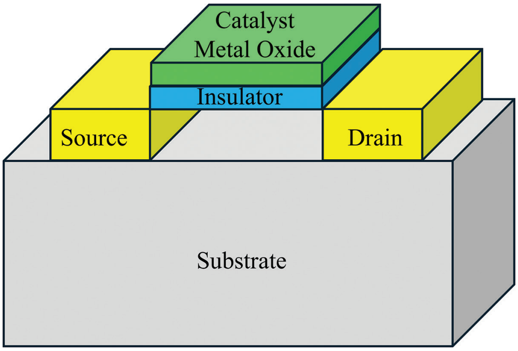


FIGURE 12.6 Catalyst-gate FET gas sensor.

12.3.3 THIN-FILM SENSOR

Thin-film sensors are advanced sensing apparatus as they do not occupy much space, usually being a few micrometers to even a fraction of a nanometer in thickness. The fabrication of these sensors employs thin-film deposition methods for construction of these highly sensitive and accurate devices. Making a thin-film sensor includes attaching electrodes for making electrical contacts and placing the thin layer of active material onto the substrate. Most sensors use metals, semiconductors, and metal oxides as their materials, but the actual material will depend on what the sensor exposes. They are selected by their ability to change physically or chemically with different gases, temperatures or light, and produce a corresponding electrical level. The great range of manufacturing methods of thin-film sensors includes such processes as sputtering, chemical/physical vapor deposition and atomic layer deposition. These methods require a different degree of accuracy, taking into consideration the thickness and the distribution of the sensor layer, to provide proper sensor operation. It becomes possible to optimize a film for its intended use as a sensor by appropriate selection of some of its features like chemical composition, shape and crystalline structure during deposition. The main aspect of thin-film sensor technology is the relationship stemming between sensor materials and external stimuli [29].

For example, metal oxide thin films (ZnO, SnO_2, TiO_2) used in gas-sensing applications change electrical resistance when faced with specific gases. The gas molecules affect the density of charge carriers and, as a result, the conductive property of the thin film by donating or withdrawing electrons away from its surface. Measuring the change can reveal the target gas's presence and concentration. Thin-film sensors' enormous surface-area-to-volume ratio allows them to pick up on even the smallest changes in their surroundings. In gas and chemical sensing, where even minute concentrations of analytes can cause significant shifts in sensor output, this feature can be extremely beneficial [30]. The structure shown in Figure 12.7 is a basic layout of the thin-film sensor.

12.3.4 CAPACITIVELY COUPLED FET

The ability to detect biological and chemical substances is facilitated by the capacitive connection between two gate electrodes in capacitor-coupled FET sensors. These sensors have a common floating gate connecting two capacitively linked gate

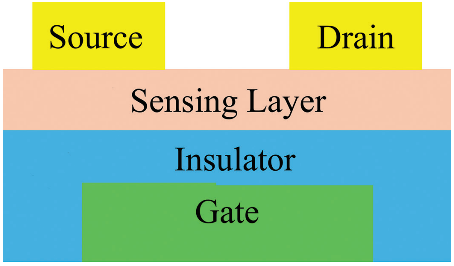


FIGURE 12.7 Thin-film gas sensor.

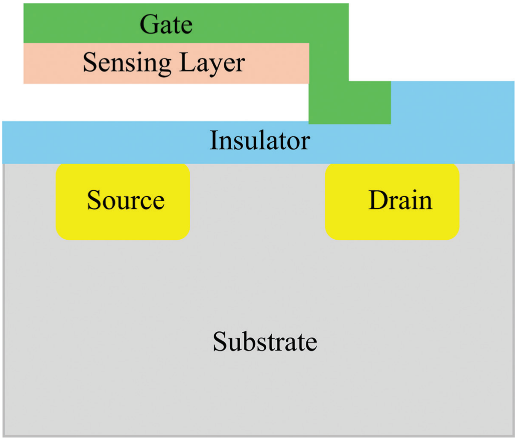


FIGURE 12.8 Capacitively coupled FET gas sensor.

electrodes. A capacitively connected FET gas sensor is made up of a FET, a capacitor, and a sensing layer with a gap of air. The FET gate is attached to a floating electrode that is one of the capacitor electrodes infused with sensing material. The opposite electrode of the capacitor, which serves as the FET's source, is well integrated and maintains a constant voltage level. The variation in sensing material's work function is the most significant factor determining the sensor's operating principle. The gas molecule's deposition on the sensor layer is what causes this fluctuation, which changes the work function of the sensing material and appears as a variation in the capacitance of the floating gate. The capacitance potential varies because the floating plate serves as both the gate electrode and the drain terminal, which alters the FET's drain current. Furthermore, the need for gas sensors that are designed with FET, such as capacitive FET sensors, because of their small size, power efficiency, high dependability, and simple fabrication process. The typical structure of capacitively coupled FET gas sensor is shown in Figure 12.8. These sensors thus provide an opportunity to devise faster means of detection and characterization of various chemicals and biological systems in their unmarked form [12].

12.3.5 HORIZONTAL FLOATING-GATE FET

Gas sensors with horizontal floating-gate FETs utilize the concept of floating-gate for detecting gas molecules in a manner similar to capacitively coupled FETs. In this case, the FET's gate has a structure that is "floating" and separated electrically, meaning it will not have direct connection to the control terminal. A sensing layer that is typically exposed to the atmosphere is connected to this floating gate. Many advantages include good sensitivity and lower operational power requirements of horizontal floating-gate FET sensors. Since minor variations in the sensor layer are capable of inducing measurable changes in the drain current, their construction permits precise gas concentration measurements. These sensors are ideal for industrial safety, environmental control, and medical diagnostics.

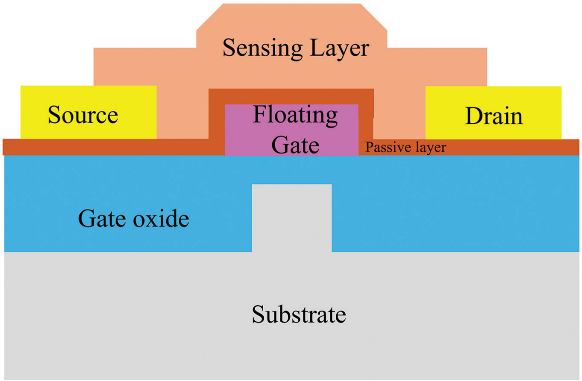


FIGURE 12.9 Horizontal floating-gate FET.

Moreover, they are quite compact in size so that it becomes easy to integrate them into any handheld gadgets [31] (Figure 12.9).

12.4 SENSING MATERIAL

Sensing material is the part in gas sensor which senses a particular type of gases present all around. Gas molecules affect the properties of a sensing material (conductivity, resistance or capacitance) and by measuring these changes with time it is possible to correlate them with gas concentrations. Below, it is a general categorization of the core types of sensing materials:

12.4.1 Metal Oxide-Based Gas Sensing

Metal oxides are metal-oxygen compounds that contain oxygen in the form of oxide ions and can have a wide range of designs and characteristics. These are probably one of the cheapest and easiest materials to make and they are very durable in oxidizing and reducing conditions and are also capable of withstanding high temperatures. Due to high semiconductive properties and high sensitivity, Metal oxide semiconductors are deemed perfect for detecting gas molecules [32].

Some of the metal oxides used in sensing of gases are the oxide of Tin (Sn), Zinc (Zn), Titanium (Ti) and Iron (Fe) since they have high sensitivity and operating temperature. These oxides exist in different crystal structures which make it possible for them to have a variety of electronic, chemical and catalytic characteristics. The activity of metal oxides in sensing gases also depends on their semiconducting characteristics which represent the change of electrical conductivity upon interaction with target gases [33] (Figures 12.10–12.12).

The existence of oxygen molecules in the operating environment is the other crucial factor for metal oxide-based gas sensors. Heat causes oxygen molecules to settle on the sensor's surface and remove electrons from the conduction band (CB), creating a depletion layer that raises the resistance of the sensor.

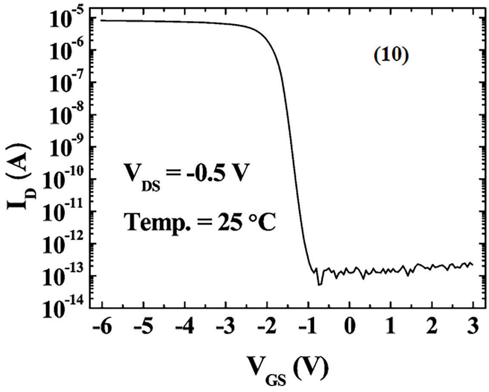


FIGURE 12.10 Transfer curve for a p-type MOSFET-based gas sensor that was fabricated at 25°C.

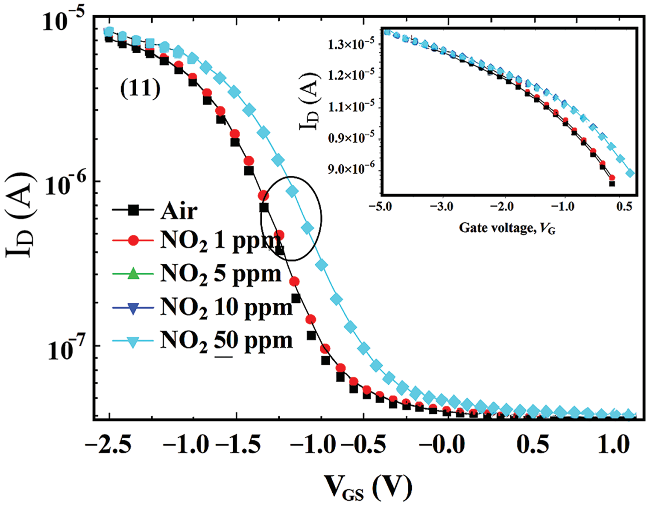


FIGURE 12.11 Transfer (I_D–V_{GS}) curves to different NO_2 concentrations.

When the adsorbed oxygen reacts with the reducing gases (carbon monoxide or methane) the electrons are restored to the material and hence the conductivity is reduced. On the other hand, there is a sharper rise of the resistance should the material come in contact with oxidizing gases such as nitrogen dioxide. These resistance changes provide the foundation for the identification of different gaseous species [35]. Due to their low price of fabrication, highly sensitivity, and because they are easy to make, they are suitable for large-scale and commercial use. They can work in harsh climate settings, including high temperatures and high humidity; this makes them ideal for use in safety measures where they try to identify tumor or combustible elements like hydrogen sulfide, methane or carbon monoxide among others.

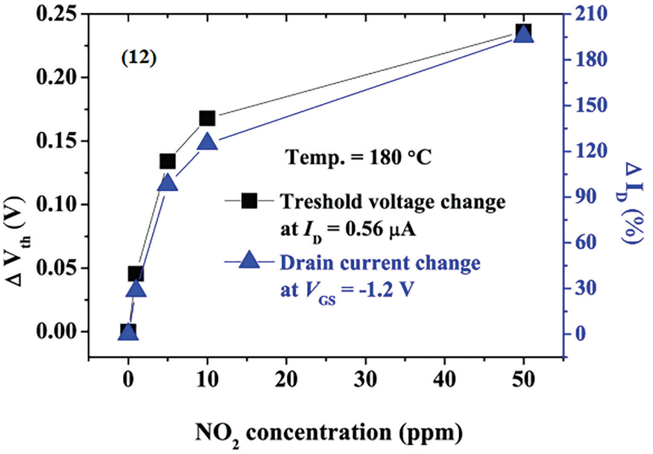


FIGURE 12.12 Variations in the built gas sensor's threshold voltage and drain current when exposed to different levels of nitrogen oxides. (Reproduced with permission from Ref. [34]. Copyright 2014, IEEE.)

Metal oxide-based sensors have comparatively higher response time to change in the concentration of the target gas. This is especially helpful where there is a need to monitor the concentrations of the gaseous compounds in real-time as in the case of monitoring of environmental pollution or air quality control systems. Also, these sensors are flexible in the sense that one can change the composition and structure of the metal oxide material, use catalysts or dopants to alter the selectivity of the sensors to particular gases.

Nonetheless, metal oxide-based gas sensors are associated with two significant challenges. The first major drawback revolves on selectivity, in that, these sensors can detect many gases and cannot distinguish between all of them in complex setting. One of the issues is stability in the case of the sensor's prolonged usage under extreme conditions or presence of contaminants, which will negatively affect the sensor's characteristics. To overcome these difficulties, recent studies have more emphasis on synthesizing nanostructured metal oxides where large exposed surface area and better adsorption characteristics of the gas are the major attracting features. To improve the developed materials' sensitivity and selectivity, a variety of morphologies including nanowires, nanotubes, and nanoparticles, have been used. Further, alloying of metal oxides with other materials, for example graphene or carbon nanotube has also been demonstrated in application of the sensors.

12.4.2 ELECTROLYTE-BASED GAS SENSING

Electrolyte-based gas sensing is a significant technology in gas sensing, with specific advantages such as extreme sensitivity, selectivity, and quick reaction to target gases. The interaction of gas molecules and an electrolyte medium produces measurable electrical changes that may be associated with the gas concentration.

In principle, the operation of electrolyte-based gas sensors is based on ion conduction between electrodes through an electrolyte with which the target gas molecules interact. This target gas that interacts with the sensor's electrolyte will cause a certain chemical reaction at one of the electrode surfaces or in the electrolyte itself. That reaction then changes the conductivity of the electrolyte or the potential difference between electrodes in some detectable and, to some degree, quantifiable manner [36].

Gas sensors that use electrolytes fall into various categories depending on the electrolyte's nature and how they work (Figures 12.13–12.16).

12.4.2.1 Solid Electrolyte Gas Sensors

These sensors make use of a solid electrolyte to move ions like O^{2-} between electrodes. Common solid electrolytes include zirconia (ZrO_2), doped ceria, or NASICON (sodium superionic conductor). Car makers often put zirconia-based sensors in oxygen sensors (lambda sensors) to measure oxygen levels in exhaust gases and optimize how engines burn fuel.

12.4.2.2 Liquid Electrolyte Gas Sensors

Some gas sensors use liquid electrolytes like sulfuric acid phosphoric acid or alkaline solutions (potassium hydroxide). These sensors play a role in electrochemical gas-sensing technologies to detect gases such as carbon dioxide (CO_2) and ammonia (NH_3). Gas molecules dissolve in the liquid electrolyte and change the ionic conductivity or pH, which creates a signal we can measure.

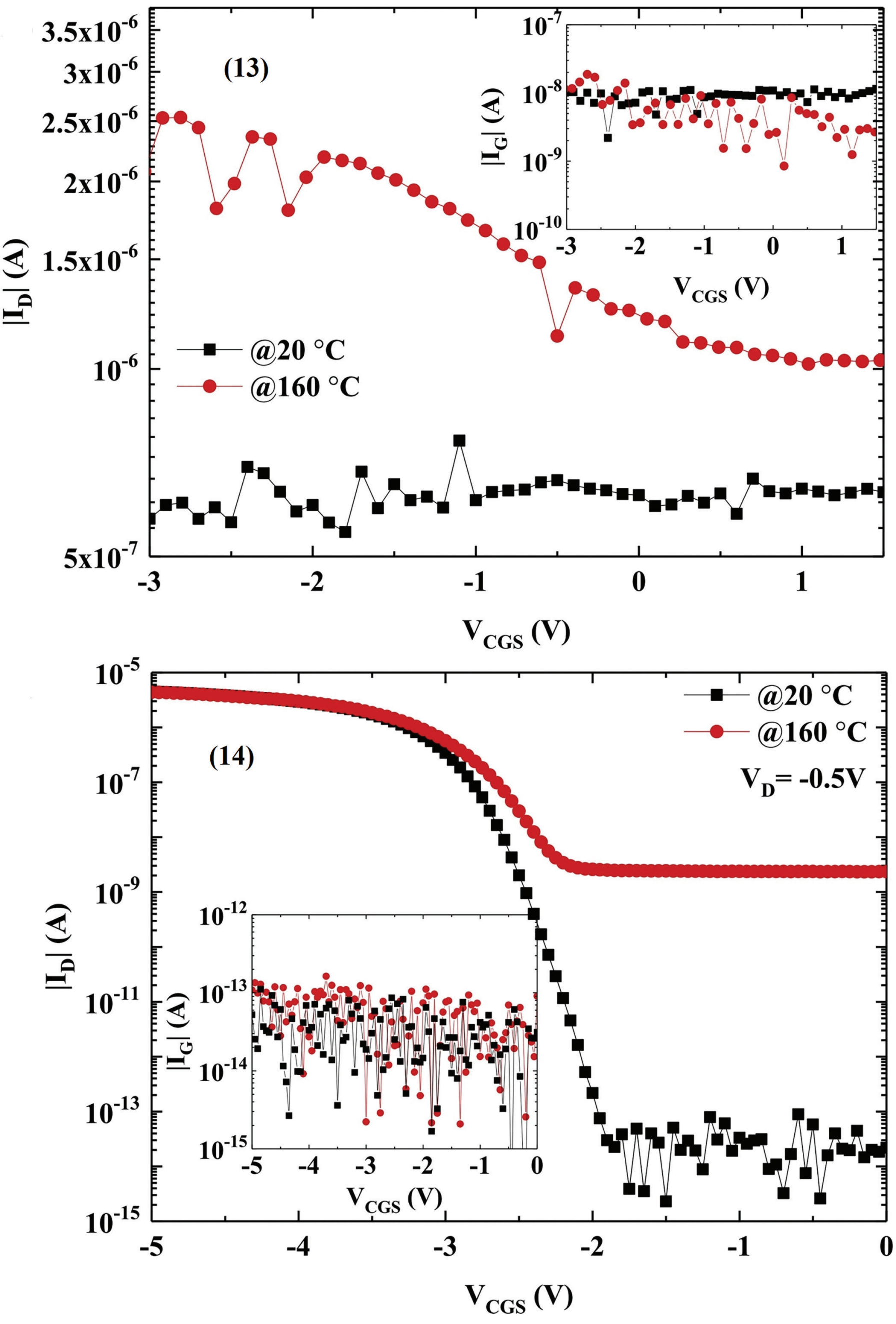
12.4.2.3 Proton-Conducting Electrolyte Sensors

Proton-conduct is sensors allow protons to move through the electrolyte when gases like hydrogen (H_2) are around. These sensors often use a proton-conducting material called Nafion®. People use them to spot hydrogen or in fuel cells. When hydrogen interacts with the electrolyte, it causes protons to shift. This movement creates an electrical signal that we can measure [37].

12.4.3 TRANSITION METAL DICHALCOGENIDES (TMDCS)–BASED GAS SENSING

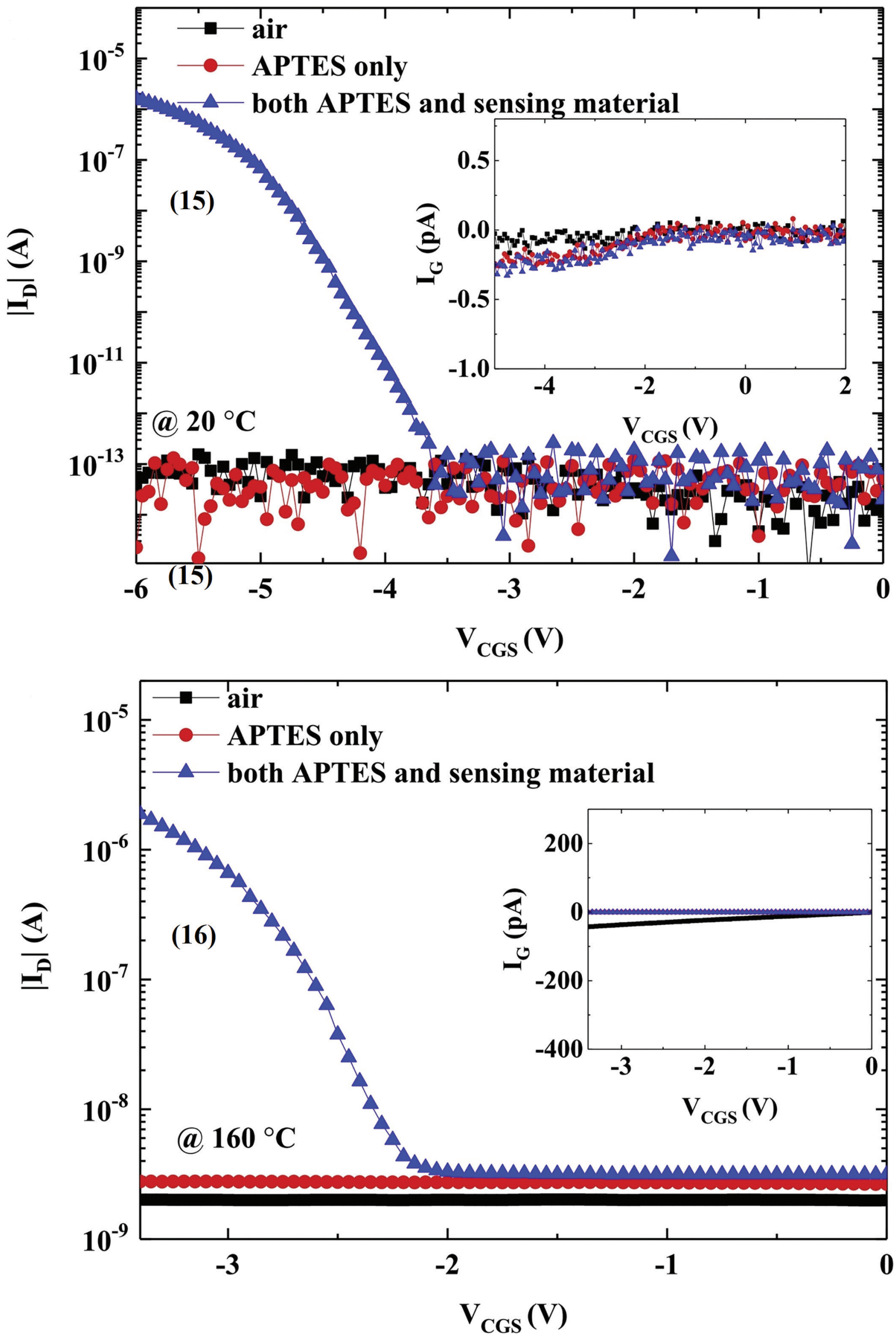
TMDCs are layered two-dimensional (2D) materials. They are made up of a transition metal split between two chalcogen atoms (like sulfur, selenium, or tellurium). Their makeup high ratio of surface-to-volume adjustable electronic features, and chemical flexibility make them great choices to detect different gases at low levels [38].

Some main TMDC materials used to sense gas are MoS_2, $MoSe_2$, WS_2, and WSe_2. They have a bandgap that engineers can adjust by varying the number of films. As an example, MoS_2 in a single layer has a direct bandgap of 1.8 eV, which is essential to develop electronic devices like FETs. This bandgap enables TMDCs to switch between conducting and insulating states when someone applies a gate voltage, which makes them perfect for FET operations. As two-dimensional materials, TMDCs have a very high ratio of surface to volume. This means every atom in the material is open to the environment. This allows gas molecules to interact a lot with

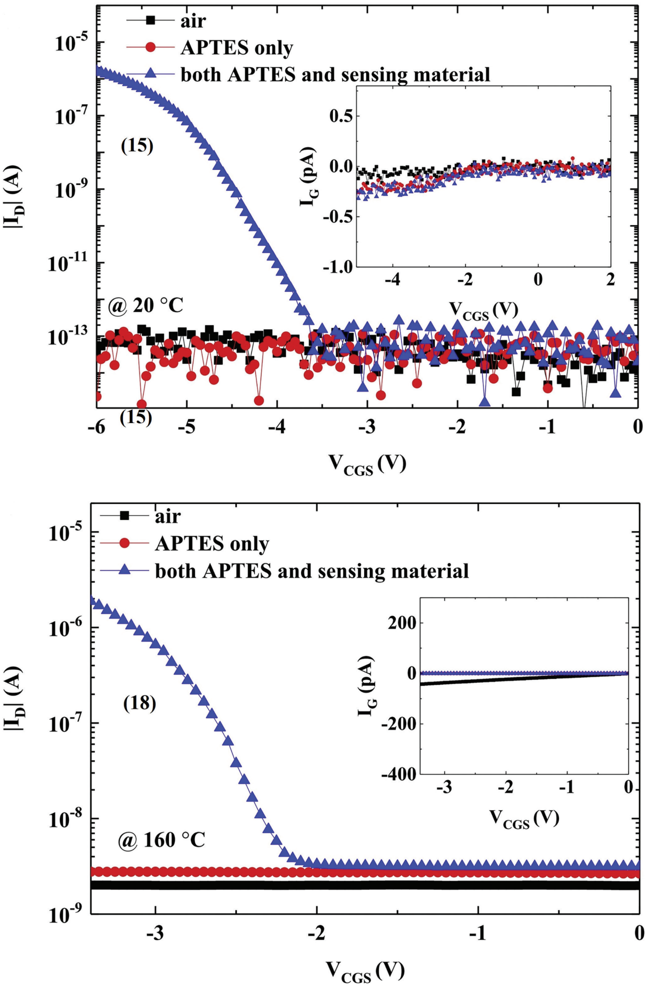


FIGURES 12.13 AND 12.14 The I_D–V_{CGS} properties demonstrate the APTES SAM's capacity to inhibit Na$^+$ ions. The I_D–V_{GS} curves are displayed in Figures 12.13 and 12.14, respectively, as a function of observed temperature (20°C and 160°C).

(*Continued*)



FIGURES 12.13 AND 12.14 (*Continued*) The I_D–V_{CGS} properties demonstrate the APTES SAM's capacity to inhibit Na^+ ions. The I_D–V_{GS} curves are displayed in Figures 12.13 and 12.14, respectively, as a function of observed temperature (20°C and 160°C).



FIGURES 12.15 AND 12.16 I_D–V_{CGS} graphs of three FET platforms with various substances (air, APTES SAM, combination of APTES SAM, and sensory material). (Reproduced with permission from Ref. [24]. Copyright 2018, Elsevier.)

the TMDC surface, which makes the material react to gas adsorption. TMDCs are active at defect sites or edges [39].

In FET-based gas sensors, the conductive channel is constructed of the gas-sensing material (TMDC) and is situated among the source terminal and drain terminal. The gate electrode changes the conductivity of the channel by varying the concentration of charge carriers across a dielectric layer. Volatile compounds adsorbed on the TMDC surface cause polarization effects within the material and alter the density of free charge carriers. Consequently, this results in a variation of the current flowing across the source terminal and drain terminal. This change in current may be observed and correlated with the gas's concentration. In TMDC based

FET gas sensors the conduit of the FET can be controlled due to adsorption of gas on TMDC surface hence this mechanism is responsible for sensing. The adsorbing gas species on the TMDC surface may increase the FET's current electronic charge or remove its negative charge, changing the FET's electrical properties. Reducing ones like H_2 and NH_3 takes away electrons from the TMDC. As a result, the channel's resistance decreases and the current increases due to the higher number of carriers in the channel. Whereas for oxidizing gases like NO_2 or O_3, the gas takes in the electrons from TMDC. As a result, there are fewer carriers in the channel, raising resistance and decreasing current [40].

Additionally, the quantity of the gas being targeted can be linked to these changes in currents. The application of gate voltage on the FET can also serve to modify the sensitivity of the sensor by controlling the charge carrier density in the TMDC layer.

12.4.4 Si-Based Gas Sensing

Due to its unique characteristics and capabilities, silicon-based gas-sensing technology has drawn the attention to several researchers. These sensors use silicon nanowires (SiNWs) and silicon nanoribbons (SiNRs) as their main sensing materials. It have an excellent ratio of surface area to volume and great electrical properties. Here are the key points about Si-based gas sensing from the given information.

Si-based gas sensors often keep the gas-sensing material apart from the conductive channel. This design helps to reduce electrical stress on the part that senses gas. As a result, the sensor lasts longer and works better. Gas molecules stick to and come off the oxide layer creating a fake gate potential. This has an impact on how well the sensor conducts electricity. As a result, the sensor responds better and is more sensitive than regular gas detectors. One key design uses SiNWs as the channel where electricity flows, with a SnO_2 film to sense gas. This setup helps detect gas well because the nanowires have a lot of surface area. Different gases make the current in the sensor go up and down. This happens because the work function of the sensing layer changes. This phenomenon is crucial for detecting different gas types and concentrations [41].

In recent years, integration of multiple gases detectors using a single microchip has become possible with recent technologies. For example, integrating both the SiNWs FETs and the film bulk acoustic resonators has been applied in differentiation between the gas mixtures that include ethanol and hexane, illustrating the use of Si-based sensors in environmental monitoring. Functionalization for Enhanced Sensitivity: Therefore, the Si-based sensors can easily be enhanced through functionalization of the chemical structures. For instance, POFs are integrated into the system to increase the sensitivity of water vapor due to their large surface area; on the other hand, PtNPs improve sensitivity of methanol vapor by enabling preconcentration of the gas [42].

Current investigations on the development of Si-based gas-sensing technologies aim at further improvement of the kind of sensors involved, better sensitivity, and new materials. There are clearly a number of probable developments that can be made in this field in the future and the areas of environmental sensing, industrial safety and personal air quality monitoring are all clearly possibilities.

12.4.5 SiC-Based Gas Sensing

Silicon carbide (SiC) has emerged as one of the most appropriate materials for use in gas sensing among a wide variety of materials because of its advantages such as high thermal stability, chemical inactivity. The first is the Shockley likeness temperature, after which carriers recombine via the direct transition, with the energy gap for the SiC polytype being found to be approximately 26 eV. These characteristics make the SiC-based gas sensors especially suitable in severe conditions, for example high temperature and corrosive atmosphere which can damage the silicon-based sensors [43].

Another advantage of SiC is versatility at higher temperature, while at high temperature other materials would simply degrade. This property enables SiC-based sensors to remain as semiconductors provided the environmental conditions are extremely harsh. Chemical stability of SiC also means that tested sensors do not degrade when exposed to corrosive gases and that is well suited for long-term stable use within gas detection applications. Thus, high sensitivity for a number of gases is possible due to increased Sic's bandgap value. This feature is especially useful in monitoring very low concentration of gases, which is vital in analysis of environment and safety [44].

The realm of gas detection has a promising new area in SiC-based gas-sensing technology. These qualities include great temperature stability, chemical inertness, and excellent sensitivity. Sic's position in gas sensing will only get stronger as a result of ongoing research and development initiatives to improve selectivity, optimize sensor performance, and integrate cutting-edge packaging technologies.

12.4.6 Gr Based Gas Sensing

Graphene (Gr) is becoming increasingly popular in gas detection applications because of its electrical conductivity, large surface area, and high mechanical strength. These characteristics make graphene a promising material for the creation sensitive gas sensors.

Graphene provides a high carrier mobility of around 200000 cm^2/Vs at room temperatures, which guarantees fast response to the detected gases. This characteristic enables the sensor to react quickly to changes in the concentration of a specific gas. The structure of graphene is extremely thin, with only one atom in thickness, and it has a large ratio of surface to volume, and thus creates a large surface on which the gas molecules can interact continually. This feature elongates the sensing capability of graphene-based sensors and enables them to distinguish even tiny amounts of gases. Since graphene is mechanically more robust, it can be incorporated into bendable electronic appliances hence can be exploited in various applications with reference to wearable sensor [45].

Graphene-based gas sensors exhibit several key performance characteristics:

Graphene sensors can achieve detection limits as low as 200 parts per billion (ppb) for certain gases, making them suitable for environmental monitoring and safety applications. Quick reaction times and recovery durations are made possible by graphene's fast charge transfer dynamics, which are crucial for real-time gas detection. By optimizing the sensing layer and employing functionalization techniques, graphene-based sensors can achieve high selectivity toward specific gases, reducing interference from other substances [46].

12.4.7 BP-BASED GAS SENSING

Nowadays, there is a lot of curiosity in using black phosphorus for gas sensing because of its qualities, which include an excellent surface quality, high carrier mobility, and an adjustable band gap. These attributes make BP suitable candidate for stability and sensitivity of the gas sensors.

Here, we introduce the properties of black phosphorus as distinct from other BP allotropes. The direct band gap of BP is present which ranges from about 0.3 to 2 eV. Therefore, by changing the total number of layers in the structure, it may be adjusted to 0 eV. Owing to this tunability, the electronic properties of the developed materials can be fashioned to suit a given gas-sensing application. BP has a puckered lattice structure whereby its surface area to volume is considerably large thus improving the gas molecules interaction with the detecting substance. This characteristic is essential in enhancing the sensitivity of the gas sensors that are present in devices [47].

The application of gas-sensing methods based on black phosphorus is a significant advancement in the discipline of gas detection. High sensitivity, fast response times, and adjustable band gaps are just a few of the unique features that make BP sensors ideal for a wide range of uses from industrial safety to environmental monitoring. BP will continue to improve its capabilities in gas-sensing applications through ongoing research focused on improving sensor performance and resolving environmental risks [48].

12.4.8 CNTS BASED GAS SENSING

Carbon nanotubes (CNTs) are being extensively studied for gas-sensing applications due to their structural, electrical, and chemical ability. single-walled carbon nanotubes (SWCNTs), like CNTs, have a large ratio of surface area to volume, especially high electrical conductivity, and outstanding mechanical properties. These characteristics give them a great sensitivity for even small concentrations of gases, This is essential to developing sensors that are extremely sensitive, quick to react and low power. This means that the interactions of gas molecules on the CNTs' surface can be identified as the fundamental mechanism of all CNT-based gas sensors. Electronic changes in synaptic transmission gas molecules that adsorb onto the CNTs modify the charge distribution along the nanotubes affecting their electrical properties, conductivity or resistance. The extent and kind of these changes depend upon the kind of gas, its concentration and whether the gas molecules behave as an electron loser or gainer. CNTs can also be incorporated into CNT-FET in which variations of the local electric field resulting from adsorbed gas affect the conductance between the source and the drain. CNT-FETs have higher sensitivity as compared to other FETs and are suitable for the detection of very low concentration of the gas [49].

Some of the parameters that make CNTs sensitive include the large surface area available in the CNTs. Relative to multi-walled carbon nanotubes, the outer surface of the SWCNTs is fully accessible for gases and fluctuations of even the lowest degree in their surroundings strongly produce observable changes in electrical signaling. Furthermore, CNTs are of 1D structure so that any surface interaction significantly affects the overall conductance was further increasing the sensitivity [50].

CNT-based gas sensors are perfect for future gas detection systems because of their high sensibility, quick response, and simplicity in size reduction. However there are issues like selectivity and stability for longer durations that are also remained hot topic for research. As the functionalization methods and the fabrication of the sensor are being improved, CNTs could be the key element for creating flexible, dependable and cost-effective gases sensing devices.

12.5 SENSING MECHANISM OF FET GAS SENSOR

A FET gas sensor's electrical properties are influenced by variations in the local electrostatic environment around the transistor's channel. This is the basis of the sensor's sensing process. The current flowing between a FET device's source and drain terminals is controlled by the voltage applied to the gate terminal. For a gas sensor, the gate is replaced or augmented by a gas-sensing material such as semiconducting nanomaterials like carbon nanotubes (CNTs), graphene, or metal oxides, which interact with gas molecules in the environment. Various mechanisms are used in FET-based gas sensor.

12.5.1 Formation of Dipole Layer

A dipole layer comes into existence when constructor gas molecules with polar attributes get adhered to the superseding sensing material. Some of the gas molecules possess a permanent dipole or can develop an induced dipole on coming in contact with the surface. The dipole moment is thus generated due to polarization within the molecule either at its basic level or by interaction with the surface of the sensor.

The direction of the dipole moment when these gas molecules are absorbed is determined by the gas's composition and degree of surface interaction. For instance, electron-deficient nitrogen dioxide (NO_2), interact with the substrate and orient the negative end on the surface. On the other hand, electron- rich species such as gases, ammonia (NH_3), will have the end of the dipole positive near the surface. It is a well-ordered array of the dipoles, which results in the formation of dipole layers: either on the side of gas or sensor material [51].

Charges at the sensor's surface are redistributed by the dipole layer in response to variations in the local density of the charge carriers (electrons or holes). For instance, if an electron-withdrawing gas such as NO_2 adsorbed, it decreased the numbers of free electrons in an n-type semiconductor or increased the number of holes in a p-type semiconductor. Since the dipole layer's development changes the sensing material's work function, this change in surface characteristics is evident. This results in a change in the work function, which is enhanced if the dipole layer is positioned perpendicular to the surface and decreased if it is lined parallel to the gas molecules' surface. They attributed these changes to the shift in work function that affects the barrier for charge injection and consequently the conductivity of the material [12].

12.5.2 SCHOTTKY BARRIER MODULATION

A Schottky barrier FET-based gas sensor is a type of gas sensor that employs the Schottky barrier modulation to improve sensitivity to a particular gas. This barrier is appropriate for use in gas sensors because it forms at the interface of a metal and a semiconductor material, and its height can be affected by surface phenomena.

The limit of electron potential energy at a metal-semiconductor contact is known as the Schottky barrier. It is worth pointing out that when metal and a semiconductor are connected, their Fermi levels get aligned, and charge carriers start to transfer to reach steady state. This results into the establishing of depletion region on the semiconductor side hence leading to formation of Schottky barrier. The motion of charge carriers across this junction is controlled by the Schottky barrier height (SBH), whose magnitude can be adjusted by restraining voltage or by surface chemisorption phenomena like gas adsorption [52].

In FET-based gas sensors the gas sensitive layer is combined with the channel layer to form a Schottky contact. Usually, metal oxides or 2D material (for example graphene) are employed for the semiconductor channel, while the electrodes are formed by metals such as platinum or gold. The target gas molecules have the ability to modify the charge density at the Schottky junction by acting as either electron donors or recipients when they come into contact with the semiconductor surface.

This causes the SBH to fluctuate upon the redistribution of charges generated by gas, which changes the carrier transport properties in the FET. As an example, electron-donating gases like ammonia (NH_3) can reduce the SBH and so boost electron transport across the channel, whereas electron-withdrawing gases such as nitrogen dioxide (NO_2) enhance the SBH and hence reduce electron transport. A signal that can be measured and corresponds to the gas concentration is then produced by the current variation reflecting itself in the FET's electrical output. This effect is most of the time enhanced in a FET structure because of the gate control and therefore making FET-based Schottky gas sensors very sensitive [53].

The FET gas sensors' great sensitivity and quick reaction are due to their ability to manipulate the Schottky barrier, which allows them to regulate the charge transport characteristics in accordance with the quantity of gas adsorbed on the surface.

12.5.3 ELECTRON DOPING EFFECT

The phenomenon of electron doping is of major significance in gas sensors that employ FET architecture; it affects their performance characteristics such as sensitivity, response time, as well as selectivity. Doping in this case means the interaction of a gas molecule with the semiconducting material in the FET channel resulting in the addition or removal of charge carriers and consequently electrics changes in the sensor. This explains the operating principle of gas sensors and their function gas quantification [54].

When gas molecules come into touch with the semiconductor material's surface, they either give away electrons or take them away from it, causing electron doping in a gas sensor based on an FET. The nature of the gas will determine if electrons are donated to the semiconductor or removed from it instead.

Electron-Donating Gases (n-type doping): Ammonia (NH_3) among other gases is quite a common example of an n-type doping gas. The sensor's semiconducting channel absorbs electrons from the adsorbed NH_3 molecules when they are introduced to the sensor's surface. As a result, the number of electrons within the material is higher than that in the absence of such gases. The rise in the number of free electrons effectively "dopes" the semiconductor by introducing more negative charge carrying carriers, thereby increasing n-type conduction. In an FET, This is seen as an increase in the current flowing across the channel between the drain and source electrodes.

Electron-Withdrawing Gases (p-type doping): On the other hand, oxygen or nitrogen dioxide (NO_2) is a common example of an electron accepting gas. When NO_2 fixes onto the surface, it takes some of the electrons that are present in the channel. Upon removal of some NO_2 molecules from the channel, ambient concentrations of free electrons become lower as some of them are now bound. p-type conduction will be more enhanced or n-type conduction will be more reversible as a result of the channel's decreased electron concentration. When applied to a semiconductor doped with n, this would result in a decrease in the current flowing through the FET channel [55].

The impact of electron doping effects varies significantly with the FET channel material employed. Conventional materials such as silicon follow stable doping behavior whereas new materials such as graphene or molybdenum disulfide or even metal oxides can provide more specific and sensitive responses. Take graphene for instance, it has a very high surface area and good conduction making induced gas electron doping very efficient. In addition, the use of nanostructured materials or nanocomposites can enhance the doping effect by improving surface activity and charge transfer processes.

12.5.4 SURFACE ABSORBED OXYGEN IONS MODULATION

Controlling the sensor's response to different gases depends on the oxygen ions that are absorbed on the outermost layer of FET gas sensors. Through their provision of active sites, these oxygen ions are in charge of gas absorption. This affects the sensor's sensitivity, selectivity, and reaction time by changing the density of charge carriers in the semiconductor channel. For this reason, enhancing FET gas sensor efficiency, particularly for the metal oxide gas sensor class represented by ZnO, SnO_2, and TiO_2, requires a good understanding and control over the behavior of the oxygen ions [56].

Let us now focus on metals and their fabrication in devices using appropriate substrates, assuming ambient air on top of the device structure and over the active layer. Surrounding oxygen gas molecules diffuse toward the interface of the molybdenum (MO) semiconductor with the air. These molecules create the anion species O^-, O_2^-, and O_2^{2-} by taking electrons from the semiconductor's conduction band. The temperature and the type of material present in the environment will affect the actual ionic species that develop. The formation of these anions in turn causes electron depletion in the vicinity of the semiconductor surfaces and creates a region which has a conductive channel but no free charge carriers [57].

12.5.5 ALTERNATING CURRENT (AC) SENSING MECHANISM

An AC sensing technique incorporated in gas sensors is based on a very advanced concept, which is a variation in any of the electrical characteristics of the gas sensors such as impedance, capacitance, conductivity etc. in existence of gas molecules on the sensor elements. When AC signal is applied to the sensor, this interaction can be assessed over time which leads to implementation of more efficient and advanced techniques of gas detection that are very high in sensitivity and selectivity. There are many benefits that come with the deployment of AC sensing compared to the DC methods, including the ability to attain higher limits of detection and effective masking of detection techniques, as well as the ability to identify gases according to their responses at different frequencies [58].

AC Sensing concentrates on the changes in potential applied across a gas sensor layer in a periodic manner and the electrical current and phase shift resulting from it. These electrical characteristics are cognate to gas interaction with the sensor material thereby altering sensor capacitance or impedance.

12.6 OPTIMIZATION STRATEGIES FOR SENSOR PERFORMANCE

FET-based gas sensors have become the focal point of researchers due to the ease of their fabrication and the inherent characteristics of the sensors like high sensitivity, low power usage and quick reaction time. Most of these sensors function by varying the current passing via a semiconductor channel whenever the gas molecules interact with the sensor surface. However, there are several applicable FET-based gas sensors which can enhance the performance metrics: the materials used, the configurations employed, and the operating conditions [59].

There are three classes of techniques that can be defined for the purpose of exploring new techniques for the sensing performances enhancement: properties of semiconductive materials, Design of sensors and mechanisms of operation oriented on enhancing sensitivity, stability and overall response time of the sensor systems.

12.6.1 FUNCTIONALITY OF SEMICONDUCTIVE MATERIALS

Gas sensors that rely on FETs are improved essentially by functionalizing their substrates. Functionalization is the practice of altering the surface of a sensor in order to improve its active interaction with target gas molecules. It can include the use of coatings, nanomaterials, or even certain chemical groups. By using this method, the adsorption of gases is improved for the sensor's use while an appropriate signal is obtained even when other gases are present and when environmental factors like temperature and humidity fluctuate. The text it concerned with the ways in which these materials may be functionalized and how this influences sensor performance [17].

Change in gas-sensing characteristics of the semiconductor surfaces can be achieved by various methods hence improving the sensitivity, stability, response period and selectivity. The following are some of the main techniques of functionalization applied in FET-based gas sensors.

Specific chemical groups are applied to the semiconductor material's surface during chemical functionalization. These groups enhance the sensor response by providing active sites for selective interaction with the gas target. These groups include for example amino groups (–NH_2), thiols (–SH) and carboxyl groups (-COOH) which help in enhancing the sensitivity, selectivity, stability and response time. Also chemical functionalization increased the selectivity of the sensor by allowing the groups to interact with the desired gas molecules only thereby inhibiting the interference of other unwanted gas molecules.

The implantation of metal or metal oxide nanoparticles to the semiconductor surface is an effective technique for increasing sensor rate. These nanoparticles serve as catalytic sites accelerating the processes of gas molecules adsorption and dissociation. Functionally, such nanoparticles may include those of Platinum (Pt), Palladium (Pd), and Gold (Au), to mention but a few. They also aid in sensor selectivity by facilitating interactions with target gases only. Nanoparticles can also enhance a sensor's sensitivity by providing more surface area for gas adsorption and helping with the gas and semiconductor charge transfer. Certain parameters such as the size, the shape, and the dispersion of the nanoparticles on the surface can be fine-tuned to improve the efficacy of the sensor.

Molecular imprinting is a method that allows the development of functional surfaces on a semiconductor by producing cavities whose shape, size, and chemical features correspond to the shape and structure of the target gas. This includes the use of gas target molecules as a template, which is infused in a polymer or inorganic material to make a reverse imprint of the gases. After the template is taken away, the gas sensor is highly selective to that particular gas [60,61].

12.6.2 SENSOR STRUCTURES

The design of gas sensors is particularly significant in defining their performance with respect to of sensibility and selectivity, reaction period, and stability, which are all considered gas sensor performance criteria. Gas sensors that use FETs primarily depend on the sensor design to decide how gas molecules interact on the detecting layer and how these interactions are converted into an electrical signal. This optimization can be further simplified into three large groups: the control of physical dimensions, engineering of the substrate and enhancement of the structure. The effectiveness of the gas detection system and the sensor's operation are greatly affected by each of these techniques.

The size of the gas sensor's active components, which includes its channel, electrodes and sensing layers, influences its sensitivity and response time. The purpose of optimizing physical dimensions is to enhance surface area of the sensor without compromising on charge carrier transport efficiency [62].

A few examples of two-dimensional (2D) materials that aid in optimizing the size of the gas sensor devices include graphene, MoS_2, and other transition metal dichalcogenides (TMDs). These materials have atomically thin layers, thereby increasing the ratio of surface area and volume, which means a larger percentage of the atoms present are involved in the interaction with gas molecules. Gas sensing can be utilized to increase sensitivity without limiting the utilization of the entire 2D material.

Increasing and optimizing the channel parameters (including length and breadth) is another crucial strategy to enhance the sensor's performance. It is clear that a shorter channel length results in a faster response time because charge diffusion among the source and drain electrodes happens more quickly. On the other hand, lowering the channel length too much would also lead to problems with contact resistance and short-channel effects. Thus, careful balancing of the channel dimensions is necessary for both high sensitivity and short response times [63].

12.6.3 OPERATING MECHANISMS

Operating regimes in gas sensing refer to the different techniques used to change the operation of a sensing element in the course of gas detection without changing the design and components of the device. Such techniques are usually concerned with the change of some external parameters such as temperature, gate bias, and exposure to ultraviolet (UV) light) for improving the sensor performance. When these operating conditions are brought to an optimum level, the gas sensor can be designed efficiently with maximum sensibility, selectivity, response period, and recovery time. This approach makes the sensor more functional, as it can work under various settings and allow for the detection of different gases without having to modify the existing sensor structure or design [64].

12.6.3.1 Temperature Control

The ability to sense gas is heavily influenced by temperature since the process of gas adsorption and desorption on the sensing material occurs at different rates depending on the temperature. This explains why in many gas sensors, especially those made from materials such as metal oxides and other semi conducting mediums, warmth is preferred so as to fasten more of the gas-surface kinetics interactions and hence more rapid and sensitive detection takes place.

Generally, at elevated temperatures, gas-phase molecules present on the surface of the sensor acquire greater energies that assist in their quick desorption when the gas is removed. This leads to shorter recovery times for the sensor. Nevertheless, too high temperature can be detrimental to the sensor, as it will desorbs so many gas molecules before they impact the sensor's electrical behavior. Consequently, it becomes important to determine temperature that would give high sensitivity and response/recovery times in the sensor.

The detection of certain gases is easier at lower temperatures. The surface of the sensor tends to absorb more gas-phase molecules at low temperatures. This increases the sensitivity of the sensor. However, this mostly leads to longer desorption times as well as longer recovery periods.

Modern gas sensors typically use micro-heaters to actively regulate the sensing area's operating temperature. These micro-heaters allow the sensor to work at different temperatures, depending on the target gas. For instance, a gas can be detected at a certain temperature for one gas and afterwards, the temperature is lowered to detect another gas. This thermal modulation improves the versatility of the sensor enabling it to detect different gases at different environmental conditions.

12.6.3.2 Gate Bias Tuning

The gate bias is one of the most crucial factors that characterizes the sensor's reaction to gas exposure. The voltage applied to a FET's gate terminal to regulate the quantity of charge carriers in the semiconductor channel is known as such gate bias. Thus, by adjusting the gate bias without physically modifying the device, it is feasible to enhance the sensor's performance by means of its sensibility, selectivity, and detection range. Gas molecules adsorbed onto a FET's semiconductor channel surface can cause a change in device's threshold voltage, just like they do with other adsorbates. Such a shift modifies the conductivity of the channel which is the sense mechanism of the gas sensor. By applying different gate bias, the threshold voltage sensitivity can be enhanced or reduced. For example, to enhance sensitivity of the sensor, it can be employed at gate voltage that is close to the threshold where even low concentration of the gas can be easy to detect. In some sophisticated FET gas sensors, two or more than two gates are involved for better performance of the sensor. In a configuration comprising of two gates, each gate can be controlled independently allowing different gases to be targeted by subjecting the different gates to different biases. This way, the operation enhances flexibility of the sensor enabling it to operate with more than one operating regime based on the gate biases arrangement.

12.6.3.3 Ultraviolet (UV) Light Activation

The gas sensor performance particularly those utilizing metal oxide, graphene and other 2D materials is known to depend quite heavily on the presence of UV light. The reason for this is that light causes excitons in semiconductors, which may then interact with the target gas molecules that are adsorbed on the surface to help sense the surrounding medium. This technique is clearly advantageous for e.g. room temperature operating sensors or for materials, which tend to be less responsive at their temperatures nearer to absolute zero.

The sensing material is activated by UV light, which causes the electrons to move from the valence band (VB) to the conduction band (CB) and gain a degree of freedom. The impact of the gas on the sensor's conductivity will either be amplified or diminished by the interaction between these excited carriers and the adsorbed gas molecules. For instance, in metal oxide-type sensors, exposure to UV light could facilitate the formation of more surface oxygen vacancies leading to preconcentration of gases such as oxygen, nitrogen dioxide.

12.6.3.4 Dynamic Operating Regimes

The rational use of operating regimes is determined by one of their most important principles, namely, the possibility of rearranging different conditions during the process of gas sensing. Instead of a single operating mode, the device can be switched between different ranges of temperature, gate bias or UV light depending on the target gas or the most important characteristics of the sensor [65,66].

12.7 FUTURE CHALLENGES AND OPPORTUNITIES FOR FET-BASED GAS SENSOR

FET-based gas sensors have attracted a lot of attention lately because of its promise for high sensitivity, low power consumption, and electronic device integration. As these sensors evolve, both challenges and opportunities present themselves in advancing their performance, scalability, and application in various industries. The foreseeable future of gas sensing with FET-based gas sensors is examined in this talk, with particular attention paid to issues such material selection, device optimization, scalability, technological integration, and the creation of cutting-edge applications.

12.7.1 Future Challenges

12.7.1.1 Selectivity

One of the most critical challenges in FET-based gas sensors is achieving high selectivity. While FET sensors are often highly sensitive to a variety of gases, distinguishing between different gases, especially in complex environments, remains a challenge. Many sensors respond similarly to various gases due to the similar electronic properties of gas molecules. This non-specific response can hinder their application in areas requiring precise gas detection, such as environmental monitoring or medical diagnostics. Different gases may produce similar changes in the sensor's electrical properties, making it difficult to accurately determine which gas is present. Humidity, temperature, and other environmental factors can also affect the sensor's performance, leading to false positives or decreased sensitivity.

12.7.1.2 Long-Term Stability and Durability

FETs have generated much attention in the development and integration of gas sensors due to their anticipated high sensitivity, low power consumption, and compatibility with other electrical components of these devices. As these gas sensors come of age, there are both obstacles and openings to surpass in further improving their quality, enhancing their availability and utilization across industries.

12.7.1.3 Response and Recovery Time

Gas sensors which utilize FET technology can provide very low response times. However, obtaining a quick recovery time which follows the sensor gets sputtered with the gas has proved to be more difficult. This is particularly so with gases that have a strong affinity to the sensing material, which makes for prolonged desorption rates. The slow recovery is not ideal and can pose challenges in deploying the sensor in real-time applications, where there is a need for continuous monitoring with a rapid reset period. For instance, in air quality monitoring systems or in industrial safety where the sensors are expected to work in air constantly.

This difficulty related to overcoming the recovery phase of gas sensors will innovation in materials or designs of operation such as UV light, heating and chemical methods, for gas desorption that will not decrease measurement performance of the sensor.

12.7.1.4 Power Consumption

Low power consumption is also critical in enhancing the practical use of gas sensors in the form of FETs in such applications as wearable devices, Internet of Things (IoT) and embedded electronics. On the other hand, it is still a challenge how to keep reduced power consumption while increasing performance. As a case, the enhancement of the motor performance of sensors often entails additional supporting circuitry, heating elements or processes such as illumination of the sensor with UV light which can be quite power hungry. To satisfy the energy requirements of today's gadgets and keep the integrity of the sensor performance, more work has to be done on designs such as energy harvesting ones, self-powered sensors and optimized micro-heaters.

12.7.1.5 Manufacturing and Scalability

The mass manufacturing of gas sensors employing FET techniques without sacrificing the precision and regularity of the sensors and devices produced is another significant challenge. A few numbers of the sensors operate on the principles of using materials at the nano scale such as highly conductive nanowires, nano tubes and or even 2D materials which are hard to produce in bulk quantity and quality. Furthermore, these sensors become even more complicated in the integration with other electronic parts and later packing them for use in practical applications in an all-weather scenario.

In order for the solution to this problem to be found it is essential that the industries apply measures like developing efficient production methods that cost less than the available ones like roll to roll fabrication, printings technologies or other methods of deposition that can produce good sensors in bulk.

12.7.2 OPPORTUNITIES

12.7.2.1 Advanced Materials and Nanostructures

The development of FET-based gas sensors will likely benefit from the ongoing search for novel materials and nanostructures. 2D semiconductors such as graphene or MoS_2, metal organic frameworks (MOFs) and perovskites are designed to impart peculiar electronic, optical and chemical functionalities that can be optimized for gas-sensing applications.

12.7.2.2 Multi-Mode Sensing

Future gas sensors may be designed with multi-mode sensing functionality, hence operating in varying environments or detecting multiple gases at once. For instance, a single FET-based gas sensor may be controlled to interface with and respond to different gases or change in the surrounding environment by varying the operating conditions such as temperature, gate bias and/or activation by ultraviolet light beam, without the need for additional sensors. Raw data processing enables the development of sensors capable of 'learning' the patterns of response for different gases at a given time thus enhancing selectivity while minimizing cross sensitivity.

12.7.2.3 Integration with IoT and Wearable Technologies

With the passage of time, there has been an increase in the need for gas sensors that are small in size, require low power, and consist of high sensitivity. FET turned gas sensors are particularly favorable for use in IoT networks due to the high miniaturization potential and low power functionalities. Such gas sensors can also be integrated into wearable devices for breathing composition measurement for health evaluation, environmental harmful gas detection as well as real-time indoor air quality assessment. Networks of FET-based gas sensors can also be established for air quality management, pollution sources detection, and providing analytics for cities in real time among other uses.

12.7.2.4 Artificial Intelligence and Machine Learning

Moreover, Artificial Intelligence (AI) and Machine Learning (ML) will be highly useful, transforming the operational capabilities of FET-based gas sensors. They can be used to classify heterogeneous information sensed using the sensor and enhance the reliability and specificity of gas sensing.

For instance, one can use machine learning algorithms to study the response of a given sensor to different operating conditions (e.g., temperature, bias) to determine the separate gases and improve gas sensor selectivity. AI solutions can be used to track the state of the sensor system and even make alerts when the sensor system is near the end of its operational life, or it requires some service change, thereby eliminating downtime and maintaining performance levels.

12.8 APPLICATION AND OUTLOOK

Gas sensors built using FET technology are now quite popular because of their design attributes, which include excellent sensitivity, quick reaction times, low power consumption, and the possibility for miniaturization. Such sensors are now finding application in many spheres including environmental monitoring, medicine, occupational health, and safety as well as in smart gadgets.

12.8.1 Environmental Monitoring

The application of FET-based gas sensors in the context of environmental pollution is one of the most promising. Real-time and accurate monitoring systems of air quality are in great current demand as air pollution shifts to be one of the most critical global issues of the end of century. Among these sensors, FET-based ones have additional benefits since they can be used to recognize even low levels of air pollutants including nitrogen dioxide (NO_2), sulfur dioxide (SO_2), ammonia (NH_3), carbon monoxide (CO), Ozone (O_3), and volatile organic compounds. FET-based sensors can be used outdoors or indoors to carry out air quality monitoring on an ongoing basis.

12.8.2 Healthcare and Medical Diagnostics

There is also a great promise of FET-based gas sensors in the field of medicine, especially when it comes to utilizing them in diagnosing diseases in a non-invasive manner. The capacity of such devices to capture particular gases from a person's breath makes it useful in healthcare since many illnesses have specific signatures detectable in breath.

12.8.3 Industrial Safety and Hazard Detection

Industrial safety is another field in which FET gas sensors have a prominent application. In this area, it is especially important to control the presence of any harmful or toxic gases in order to minimize the risk of accidents as well as safeguard the health of the workers. The chemical industry, particularly chemical manufacturing, mining, and oil and gas extraction involve the use of processes that frequently emit harmful gases which endanger health and safety. For example, Additionally, FET-based sensors may be used for evaluating the concentrations of dangerous gases, including as CO, H_2S, and NH_3, which are commonly present in industries. Such sensors may be placed in plants, petrol drying cabinets, or even thermal processing plants for persistent assessment of gas leaks or the increase of hazardous gas volumes within the environment to raise alarm and avert disaster occurrence.

12.8.4 Smart Devices and Consumer Electronics

The integration of gas sensors based on FETs into consumer electronics and smart devices is an area that is rapidly gaining interest. With the expansion of smart home technology, there is a growing need for sensors that can keep track of the air quality, detect any poisonous gases, and feedback to users in real-time. Suitable FET-based gas sensors can be commercially deployed in smart homes system in evaluating the air quality within the house. Such sensors can also monitor the presence of domestic irritants and pollutants such as VOCs, CO and Formaldehyde in quite a respective time to the householders.

12.8.5 Automotive Industry

FET-based gas sensors offer excellent potential in the automotive industry as well. FET-related sensors can also be employed to measure the exhaust gases emitted from automobiles, thus assisting in maintaining the emission levels within the prescribed limits of any environmentally friendly regulations. These gases may include nitrogen oxide (NO_2) and carbon (CO) which are a few of the controlled emissions gases, thus while an automobile is in operation these sensors can also monitor the emissions and implement countermeasures if the emission levels are exceeded.

12.9 CONCLUSION

FET-based gas-sensing technologies have indeed progressed remarkably over the years and hold tremendous prospects for the innumerable applications they can have in the future. With research continuing to address existing challenges, the future of FETs for gas detection has good promise for various industries providing safer, efficient and greener ways of monitoring and analyzing gases. Evolving as one of the top technologies for environmental and public safety applications in the years to come, it is expected that these sensors will play a major role.

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13 High-Performance Silicon Nitride Waveguides

A Platform for Nonlinear and Quantum Photonics

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LEARNING OBJECTIVES/KEY POINTS

1. SiN waveguides offer low optical losses, making them ideal for high-performance photonic devices and communication systems.
2. The high refractive index contrast between SiN and the cladding allows for efficient mode confinement, enabling compact waveguide designs with minimal optical leakage.
3. SiN waveguides can be fabricated using standard complementary metal-oxide-semiconductor (CMOS)-compatible processes, enabling cost-effective manufacturing and integration with existing silicon photonics technologies.
4. The study of waveguide geometry (such as thickness and width) is crucial for optimizing performance, balancing trade-offs between confinement, loss, and scalability in integrated photonics.
5. Numerical tools such as FDTD (Finite-Difference Time Domain) and eigen-mode solvers are used to model and optimize SiN waveguides for specific applications, ensuring precise performance predictions before fabrication.

13.1 INTRODUCTION

Silicon nitride (SiN) waveguides constitute a multifaceted photonic platform that has achieved extensive application in integrated optics, quantum technologies, and optical communication. They are esteemed for their little transmission loss, extensive transparency range, and compatibility with complementary metal-oxide-semiconductor (CMOS) processing, rendering them appropriate for mass production and integration with current silicon photonic systems. SiN exhibits transparency across a wide spectrum of wavelengths, spanning from visible light to mid-infrared (400 nm to 7 µm) [1]. This spectrum encompasses visible, near-infrared, and portions of the mid-infrared range, facilitating applications across several domains, including visible-region quantum technologies, optical communication notably at 850 and 1550 nm, and biological sensing. SiN waveguides exhibit minimal optical losses (generally

DOI: 10.1201/9781003543923-13

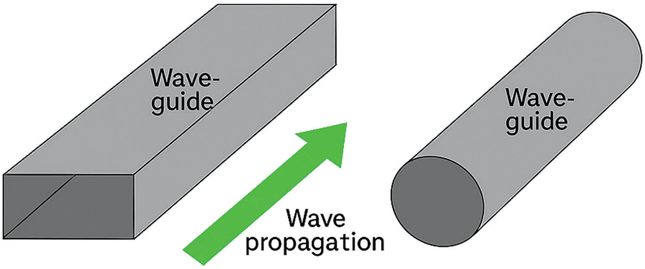

FIGURE 13.1 Schematic of different waveguide [1].

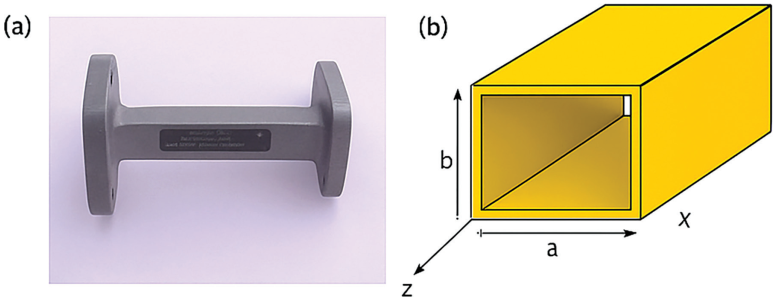

FIGURE 13.2 Structure and dimension of rectangular waveguide [1].

<1 dB/cm under optimum conditions), particularly in the visible and near-infrared spectra. The little loss renders them appropriate for long-distance signal transmission on a chip, advantageous for applications necessitating high-performance, long-range waveguiding. SiN possesses a refractive index (~2.0) that exceeds that of silicon dioxide (~1.45), facilitating robust mode confinement within the core [2]. Figure 13.1 specifies schematic of different waveguide structure.

SiN waveguides can be manufactured with conventional CMOS methods, enhancing their economic viability. This compatibility enables monolithic integration with silicon-based electronic and photonic components, promoting the advancement of hybrid photonic circuits. The mode profile in a waveguide describes the spatial distribution of the electric and magnetic field intensities within the waveguide's cross-section [3]. It represents how light propagates through the waveguide and is determined by the waveguide's geometry, refractive index contrast, and wavelength of operation. Figure 13.2 represents structure and dimension of rectangular waveguide.

The mode profile illustrates the extent to which the field is contained within the waveguide core compared to the amount that permeates into the cladding. An effectively engineered mode profile must exhibit robust confinement inside the core, hence reducing leakage and scattering at the peripheries. This distribution directly influences coupling efficiency, propagation loss, and interactions with other photonic components. Each mode possesses an effective refractive index, indicating the extent to which the waveguide construction alters light propagation inside it [4]. The effective index is contingent upon wavelength and waveguide geometry, affecting the

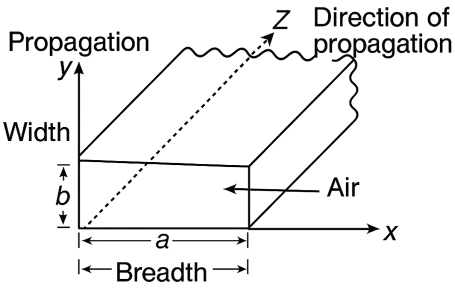

FIGURE 13.3 Wave propagation direction in waveguide [3].

waveguide's dispersion characteristics, particularly in applications such as frequency combs and nonlinear optics. Mode profile simulation, which matches mode shapes, ensures appropriate coupling for devices such as quantum emitters and free-space optical systems. Mode converters must be designed and integrated with external systems such as fibers or detectors to function properly. Figure 13.3 represents wave propagation in waveguide.

Plays a key role in the study of dispersion relations and chromatic dispersion, both essential for enabling high-speed optical communication. Accurate mode profile simulations help develop dispersion-engineered waveguides for broadband operation. Mode profile simulations in quantum photonics provide effective overlap between the guided mode and the quantum emitter, which improves light-matter interactions [5]. It is critical for optimizing the Purcell effect in optical cavities integrated with waveguides. Waveguide guides light with little loss over long distances or within compact integrated photonic circuits. It maintains the integrity of the optical signal while preventing diffraction and scattering. To obtain high power density while minimizing interaction with undesirable regions, confine light to certain dimensions. Waveguides in optics connect light generation, manipulation, and detection. Their objectives and scope range from fundamental research to cutting-edge applications in quantum communication, optical computing, sensing, and beyond. Your work merging waveguides with quantum devices is directly related to the advancement of these domains, notably next-generation optical communication and quantum technology.

13.1.1 THEORY AND PRINCIPLES OF WAVEGUIDE MODES

As the foundation of optical systems, waveguides have aims that can be broadly divided into three categories: functional, technological, and application-specific. Mode profile simulations improve light-matter interaction in quantum photonics by guaranteeing efficient overlap between the guided mode and the quantum emitter essential for maximizing the Purcell effect in waveguide-integrated optical cavities. By distinguishing between transverse electric (TE), transverse magnetic (TM), or hybrid modes, simulations can make sure the design satisfies polarization-specific specifications. Mode simulations in taper or bending waveguides aid in loss prediction and device compactness optimization. Mode simulations in taper or bending waveguides aid in loss prediction and device compactness optimization [6].

The SiN (Si_3N_4) planar waveguide platform has facilitated the development of a wide range of low-loss, planar-integrated devices and chip-scale solutions. Figure 13.4 represents distribution of electromagnetic waves (EM) waves.

This platform is advantageous due to its broad wavelength transparency. Low-loss waveguides (<1 dB/m) capable of handling high optical power can be tailored for both linear and nonlinear optical functionalities, supporting diverse passive and active components. This versatility unlocks new possibilities for system-on-chip implementations. As signal bandwidth and data rates grow, the advanced optical circuit functionalities enabled by Si_3N_4 have broadened the scope of practical applications in optical signal processing [7]. Figure 13.5 depicts EM wave propagation in waveguide.

Si_3N_4 photonic integrated circuit (PIC) technology provides exceptionally low optical attenuation across a broad spectrum, spanning from the visible to beyond the infrared—a range unmatched by other platforms. Si_3N_4 PIC technology offers lower-loss waveguides and building blocks that complement silicon-on-insulator (SOI) and III–V PIC platforms. Traditionally, Si_3N_4 has been employed in standard CMOS processes for insulating individual transistors through the local oxidation of

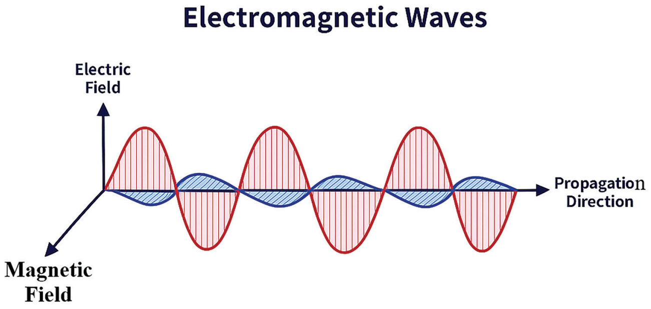
Electromagnetic Waves
Electric Field
Propagation Direction
Magnetic Field

FIGURE 13.4 Distribution of EM waves [3].

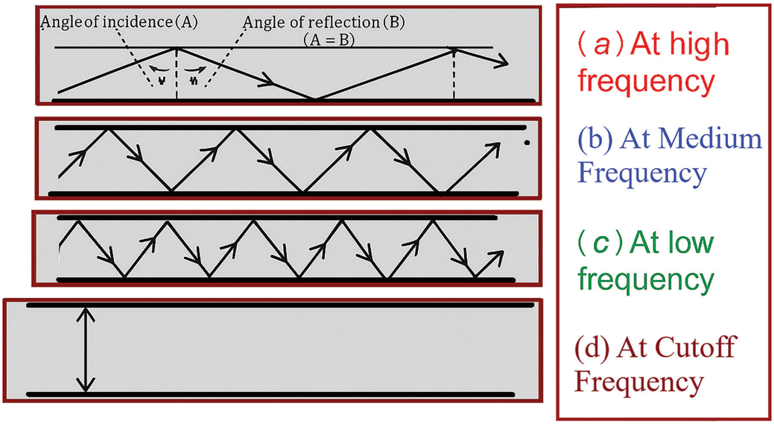
Angle of incidence (A)
Angle of reflection (B)
(A = B)
(a) At high frequency
(b) At Medium Frequency
(c) At low frequency
(d) At Cutoff Frequency

FIGURE 13.5 EM wave propagation in waveguide [4].

silicon (LOCOS) technique and as a gate material in ion-sensitive field-effect transistors (ISFETs) [8]. Optical waveguides feature a Si_3N_4 core layer embedded within a silicon dioxide (SiO_2) cladding. At a wavelength of 1.55 µm, the refractive index of the cladding (1.45 for SiO_2) and the core (1.98 for Si_3N_4) enables the design of waveguides with varying refractive index contrast. These waveguides exhibit low propagation losses, ranging from approximately 0.3–1.0 dB/cm, across a broad wavelength spectrum of ~400–2350 nm [9].

13.1.2 BACKGROUND OF Si_3N_4 WAVEGUIDE

Given the limitations of traditional waveguides, researchers have focused on exploring new materials. SiN has emerged as a promising platform due to its compatibility with CMOS technology and broad application potential. With an optical band gap of approximately 5.1 eV, it offers a transparent window spanning from the visible to the mid-infrared range. Additionally, under high-power conditions, SiN does not exhibit two-photon absorption, helping to minimize absorption losses in waveguides. Although the refractive index of SiN (~2.0) is lower than that of silicon (~3.47), which requires a wider single-mode waveguide, it also enhances processing error tolerance [9]. SiN is an excellent epitaxial material, enabling integration with other systems for high-performance 3D photonic devices. As a result, high-quality SiN films are well suited for use as the core layer in waveguide devices. Figure 13.6 represents different configurations of waveguide.

SiN photonics has enabled a diverse range of low-loss integrated devices and chip-scale solutions, leveraging its wide wavelength transparency and compatibility

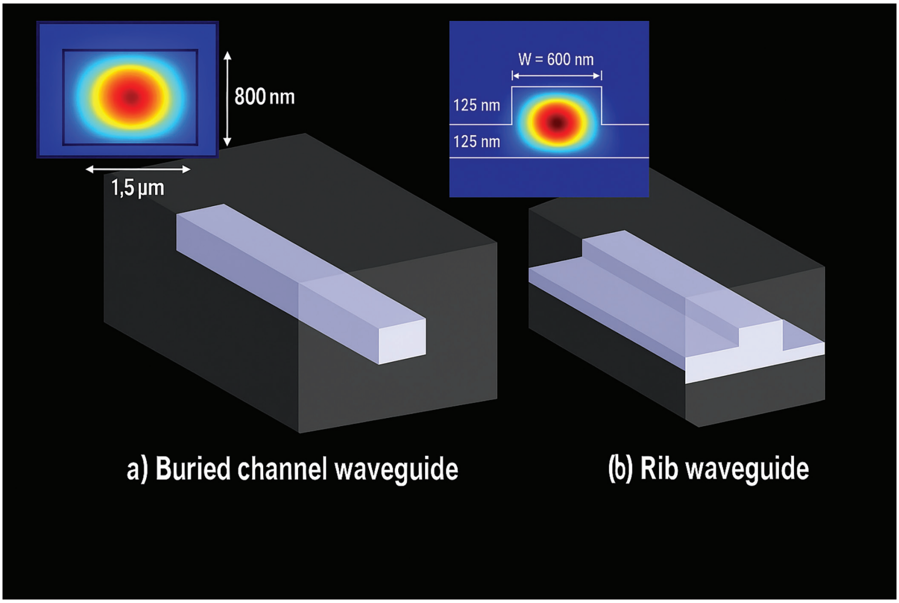

FIGURE 13.6 Different configuration of waveguide structure [5].

with CMOS processes. This versatility supports applications in telecommunications, data communications, artificial intelligence, sensing, and biophotonics. As a complementary platform to SOI photonics, low-loss SiN waveguide technology enhances the capabilities of the silicon photonics platform. SiN films prepared through low-pressure chemical vapor deposition (LPCVD) offer low intrinsic loss and high repeatability but are prone to cracking when their thickness exceeds 300 nm [10]. To address this issue, 400-nm-thick wafer-scale SiN waveguides were successfully fabricated using a two-step deposition method on 200-mm CMOS-compatible wafers. Thermally oxidized silica is among the lowest-loss oxide-based cladding materials, attributed to its low surface roughness derived from the high-quality silicon substrate and the absence of hydrogen in the material and growth process. The higher-index waveguide core is typically fabricated using chemical vapor deposition (CVD), followed by patterning and etching to create channel waveguides. Early designs featured an air upper cladding, but later advancements introduced deposited oxide upper claddings to mitigate losses caused by surface roughness, lithography-induced scattering, and material optical absorption [10]. The thickness of the thermally grown lower cladding layer must be adequately large, typically ranging from several micrometers to 15 μm, to reduce absorption in the silicon substrate. The required thickness depends on the level of optical waveguide confinement.

A broad array of 1550-nm telecommunication devices based on SiOxNy, including filters, polarization splitters, fiber-to-waveguide mode transformers, tunable optical add/drop multiplexers, thermally controlled optical switches, and bus-coupled ring resonators, have been successfully demonstrated. High aspect ratio Si_3N_4 cores with a 40-nm-thick Si_3N_4 core were used to minimize sidewall scattering. A thin conformal layer of LPCVD was deposited over the etched waveguides and then planarized using chemical mechanical polishing (CMP). The thermally grown oxide upper cladding layer was wafer-bonded to the planarized LPCVD layer to reduce absorption losses and other loss mechanisms associated with deposited oxide films. These waveguides supported high optical power with minimal induced nonlinear optical phase shifts, as well as highly selective single-mode TE polarization propagation, exhibiting over 75 dB of TM loss relative to TE polarization [11].

13.1.3 Si_3N_4 TECHNOLOGY AND PLATFORM

Waveguides are typically fabricated on highly flat substrates, such as single-crystal silicon. For applications requiring transparency in the visible light region, fused silica glass substrates are often used. The stripe waveguide geometries consist of an alternating layer stack of SiO_2 cladding layers and Si_3N_4 core layers. The high-index waveguide core is created using deposition techniques such as chemical vapor deposition (CVD), followed by patterning and etching processes to shape the channel waveguides. One of the earliest reported silicon nitride/silicon dioxide (Si_3N_4/SiO_2) waveguides was a single-mode channel waveguide [9] with a propagation loss of 1–2 dB/cm [12]. These early losses were comparable to the performance of modern state-of-the-art SOI waveguides, which exhibit losses of approximately 0.3 dB/cm, and optical fibers with a record loss of 0.4160 dB/km. A wide range of SiOxNy 1550-nm telecommunications devices including filters, polarization

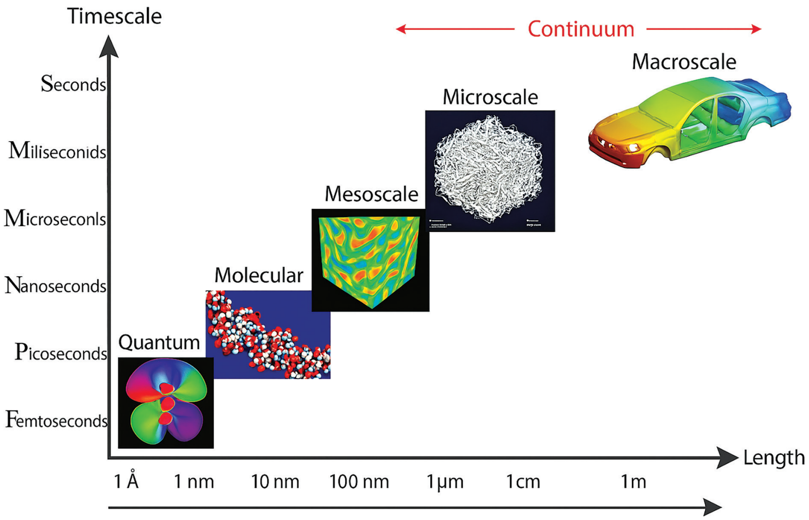

FIGURE 13.7 Trade-off in Quantum technology [6].

splitters, fiber-to-waveguide mode transformers, tunable optical add/drop multiplexers, thermally controlled optical switches, and bus-coupled ring resonators were demonstrated [12]. A thin conformal LPCVD layer was deposited over the etched waveguides and then planarized using chemical mechanical polishing (CMP). To minimize absorption losses and other loss mechanisms associated with deposited oxide films, a thermally grown oxide upper cladding layer was wafer-bonded to the planarized LPCVD layer. Figure 13.7 shows trade-off in quantum technology.

Propagation loss primarily consists of absorption loss, radiation loss, and scattering loss. Due to the limitations of current CMOS technology, the sidewalls of the waveguide tend to be relatively rough, resulting in scattering losses as light propagates through the waveguide. Among these factors, scattering loss predominantly contributes to the overall propagation loss [13].

To address this, a 3D modeling approach based on Fourier transform and finite-difference time-domain (FDTD) methods has been employed [12]. This method enables precise analysis of the impact of sidewall roughness on the propagation loss of optical waveguides. The FDTD simulations provide valuable insights to support the fabrication process. In the simulation, the light source operates at a wavelength of 1550 nm, with energy monitors positioned at both ends of the waveguide to measure performance [14]. The pursuit of compact Si_3N_4 devices and enhanced mode confinement for efficient optical nonlinear interactions prompted researchers to develop technologies and processing techniques for thick nitride waveguides ranging from 600 nm to 6.5 µm. The waveguide loss, resonator quality factor (Q), and free spectral range (FSR) are influenced by changes in core thickness. In straight waveguides and those with moderate to large bend radii, losses are primarily caused by sidewall scattering of the core. However, when the bend radius falls below a critical value, bend losses become dominant. For a fixed waveguide width and core thickness, designing bends with radii above this critical value minimizes losses [15].

When the optical mode diameter roughly matches the core width, the waveguide operates in the high-confinement regime. As the core width decreases, the optical mode diameter expands rapidly, entering the squeezed-out regime. By selecting the appropriate core thickness, a PIC designer can balance loss and its sensitivity to the device footprint, transitioning between bend loss-limited and scattering loss-limited regimes as needed. Single-mode waveguide resonators have achieved quality factors (*Q*) as high as 30 million, with propagation losses of approximately 0.5 dB/m [16].

13.1.3.1 Capabilities and Implementations

The applications extend from the visible wavelength range to the mid-infrared (MIR), covering a diverse array of fields including communications, sensing, and biophotonics. The infrared range (1.0–2.3 µm) benefits from its transparency, low loss, and the ability to co-package Si_3N_4 circuits with SOI and indium phosphide(InP). Applications in this range include lasers, optical filters, delay lines, true time delays, optical signal processors, and optical frequency comb generation. In the visible (400–700 nm) and near-infrared (700–1000 nm) wavebands, Si_3N_4 complements the capabilities of SOI photonics.

External cavity lasers typically combine semiconductor optical amplifiers (SOAs) or gain blocks with external high-Q discrete components, such as fiber Bragg gratings (FBGs), to create tunable sources with fundamental linewidths as narrow as 15 Hz. This level of performance has the potential to be achieved on-chip using Si_3N_4 high-Q resonators or long sidewall etched gratings. A compact hybrid laser with an integral linewidth of 13 kHz was demonstrated, featuring an InP gain block coupled to a high-Q Si_3N_4 microring resonator (MRR) as the external laser mirror. Microlasers emitting at 630 nm utilize colloidal quantum dots positioned between two Si_3N_4 resonator layers and coupled to an Si_3N_4 waveguide [17].

13.2 DEVICE DESIGN AND METHODOLOGY

We theoretically investigate the potential of the Si_3N_4-on-SiO_2 waveguide platform for wideband spectroscopic detection near the 2 µm optical wavelength. The study focuses on designing Si_3N_4-on-SiO_2 waveguide architectures, including an Si_3N_4 slot waveguide for wideband on-chip spectroscopic sensing around 2 µm, and a Si_3N_4 multimode interferometer (MMI)-based coupler for efficient light coupling from a classical strip waveguide into the Si_3N_4 slot waveguides over a broad spectral range. At shorter optical wavelengths, the optical field of the quasi-TE mode is more concentrated in the two side regions of the waveguide [18]. As the wavelength increases, the field gradually shifts toward the central region of the slot waveguide. However, from a 3D perspective, it may be more challenging to observe the subtle shift of the optical field (evanescent field) that extends into the substrate at longer wavelengths. Figure 13.8 depicts the proposed structure of Si_3N_4 waveguide.

For on-chip signal transmission via a silicon microring, the signal wavelength is tuned to match the microring resonance to prevent unwanted filtering effects, as the microring exhibits a narrow bandwidth. In contrast, a silicon strip waveguide,

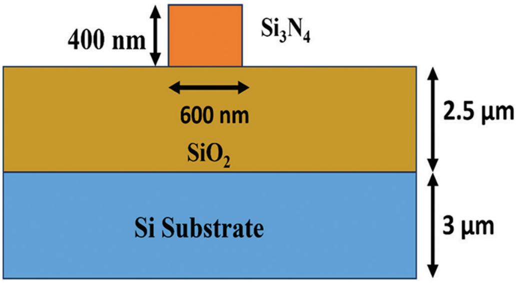

FIGURE 13.8 Proposed structure for Si_3N_4 waveguide.

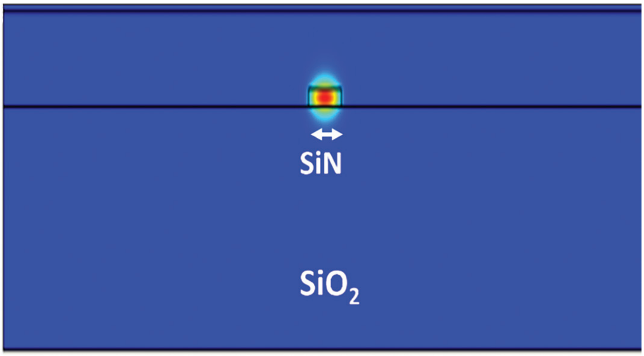

FIGURE 13.9 Simulated structure for Si_3N_4 waveguide.

without a microring configuration, offers broad transmission bandwidth. The slot waveguide, an advanced version of the strip waveguide, reduces nonlinearity by confining light within its low-index air slot region. Consequently, we design and fabricate a silicon slot waveguide to enable broadband signal transmission on-chip.

Figure 13.9 depicts simulated structure of waveguide. The structure comprises three main components: a mode converter for strip-to-slot conversion, a slot waveguide, and another mode converter for slot-to-strip conversion. The air slot region has a width of 100 nm and a height of 220 nm. The mode converter introduces a loss of approximately 0.5 dB, while the slot waveguide exhibits a propagation loss of 5 dB/cm, primarily due to the roughness of the slot sidewalls. On-chip signal transmission is analyzed for different waveguide lengths. The bit error rate performance of on-chip signal transmission is evaluated using four different lengths of the silicon slot waveguide.

First, the SiN layer was deposited to the desired thickness using Plasma-Enhanced Chemical Vapor Deposition (PECVD) on a 4-inch silicon substrate with a 5 µm silicon dioxide (SiO_2) BOX layer, obtained via wet thermal oxidation. The deposition process utilized a gas mixture of 5% SiH_4 diluted in N_2 (600 sccm) and pure NH_3 (16 sccm) [19]. The deposition was conducted at a process temperature of 400°C and a pressure of 1200 mTorr. The plasma frequencies alternated between high frequency (13.56 MHz) and low frequency (100 kHz), both operating at 50 W power, with durations of 13 and 7 seconds, respectively.

The optimized deposition parameters ensure a SiN film with excellent optical quality and uniformity. Ellipsometry measurements revealed that the refractive index of the deposited film is 2.01 at a wavelength of 1550 nm. In the next step, an 800-nm-thick layer of positive photoresist was spin-coated onto the wafer and cured. The waveguide patterns were defined using a high-quality contact mask in conjunction with a contact mask aligner (MA6, Karl Suss), with the i-line source intensity set to 5.0 mW/cm² [9]. Following the development and hard-bake process, the pattern from the photoresist was transferred to the SiN layer using reactive ion etching (RIE), thereby forming the waveguide core structures.

13.2.1 SIMULATION METHODOLOGY

Numerical simulations indicate that the waveguide dimensions support only the fundamental TE and TM modes, with the loss measurements conducted under TE polarization. Notably, an intrinsic absorption band is observed around 1525 nm, particularly in longer spiral waveguides. This absorption band extends up to 1595 nm, spanning a bandwidth of over 70 nm. The origin of this absorption is attributed to the second overtone of the N-H stretching vibration [20].

A potent numerical method for resolving electromagnetic issues is the Finite Element Method (FEM), especially in intricate geometries like waveguides. When FEM is used in waveguide analysis, the waveguide structure is discretized into smaller, more manageable components. Maxwell's equations are then solved within each element, and the global answer is then put together [21].

$$\nabla x\vec{E} = -jw\mu\vec{H} \tag{13.1}$$

$$\nabla x\vec{H} = jw\mu\vec{E} \tag{13.2}$$

$$\nabla_t^2\overrightarrow{E_t} + \left(\beta^2 - k_0^2\right)\overrightarrow{E_t} = 0 \tag{13.3}$$

$$\overrightarrow{E_t}\left(x, y\right) = \sum_i \overrightarrow{E_i} N_i\left(x, y\right) \tag{13.4}$$

$$\frac{\partial^2 E_y}{\partial x^2} + \left(k^2 - \beta^2\right)E_y = 0 \tag{13.5}$$

$$k^2 = w^2\mu_0 E\left(x\right) \tag{13.6}$$

$$\frac{\partial^2 H_y}{\partial x^2} + \left(k^2 - \beta^2\right)H_y = \frac{1}{\in}\frac{dE}{dx}\frac{\partial H_y}{\partial x} \tag{13.7}$$

$$H_x = \frac{-\beta}{w\mu_0} E \tag{13.8}$$

$$H_z = \frac{1}{iw\mu_0} \frac{\partial E_y}{\partial x} \tag{13.9}$$

$$E_x = \frac{\beta}{w \in} H_y \tag{13.10}$$

$$E_z = \frac{-1}{iw \in} \frac{\partial H_y}{\partial x} \tag{13.11}$$

The FEM is a robust numerical technique used to analyze waveguides by solving Maxwell's equations in complex geometries. It involves discretizing the computational domain into smaller finite elements, such as triangles in 2D or tetrahedra in 3D, allowing precise modeling of waveguide structures, including the core, cladding, and substrate. FEM solves the vector wave equation for the electric field, reformulating it into a matrix eigenvalue problem to compute propagation constants and field distributions. Boundary conditions, such as Perfectly Matched Layers (PML), are applied to mimic open systems and avoid reflections. The effective refractive index and mode profiles are obtained from the eigenvalue solutions, enabling detailed analysis of mode confinement, propagation characteristics, and loss mechanisms [22]. FEM is particularly advantageous for waveguides with irregular geometries or high-index contrast and is widely used in the design of integrated photonic devices.

Wavelength selection in SiN waveguides, including the commonly used 1550 nm telecommunication wavelength, plays a crucial role in photonic applications. SiN is highly versatile due to its wide transparency window, covering wavelengths from the visible to the mid-infrared (400 nm to 7 μm), making it suitable for diverse applications such as optical communication, nonlinear optics, and biosensing [22]. The 1550 nm wavelength is particularly significant due to its low loss in optical fibers, enabling efficient coupling and integration with fiber networks. SiN waveguides at 1550 nm also exhibit low propagation losses, typically below 1 dB/cm, when optimized, thanks to their excellent material properties and reduced two-photon absorption compared to silicon. Furthermore, the high-index contrast between SiN and SiO_2 ensures tight mode confinement, allowing for compact device designs. This wavelength is also ideal for leveraging the low dispersion characteristics of SiN, making it suitable for broadband and high-speed optical circuits.

13.3 RESULTS AND DISCUSSION

The mode profiles in SiN waveguides are critical for understanding their optical performance and guiding behavior. The fundamental mode, typically the TE_{000} or TM_{000} mode, exhibits strong confinement within the SiN core due to the high refractive index contrast between SiN and its surrounding cladding materials, such as SiO_2. These modes have a well-defined, symmetric electric field distribution, making them highly desirable for low-loss and efficient optical transmission. Higher-order modes, such as TE_{111} or TM_{111}, appear when the waveguide dimensions exceed the cutoff condition for single-mode operation. These modes have more complex field distributions, often with multiple intensity peaks across the waveguide cross-section. The presence of higher-order modes can lead to mode coupling or dispersion, impacting device performance. Numerical simulations, such as those using the FEM, are employed to visualize these mode profiles and calculate their effective refractive indices, confinement factors, and cutoff wavelengths. For optimal device design, SiN waveguides are often engineered to operate in the single-mode regime, ensuring robust light propagation while minimizing crosstalk and higher-order mode interference. Figure 13.10 depicts the mode profile of Si_3N_4 waveguide.

The analysis of effective refractive indices in SiN waveguides is essential for evaluating their guiding characteristics and mode confinement efficiency. Neff depends on the waveguide geometry, material refractive indices, and the operating wavelength. For a given wavelength, the effective index is higher for tightly confined fundamental modes due to the stronger overlap of the optical field with the high-index SiN core. Higher-order modes, when supported, exhibit lower effective indices, as their fields extend further into the lower-index cladding, reducing mode confinement. Numerical methods, such as the FEM or finite-difference eigenmode (FDE) solver, are typically employed to calculate neff for different waveguide dimensions and refractive index profiles. Variations in neff across wavelengths can reveal chromatic dispersion, which is a critical parameter for broadband applications. Precise control and characterization of neff enable the design of waveguides optimized for single-mode operation, efficient coupling to external optical systems, and low propagation losses, thereby enhancing the performance of photonic integrated circuits based on SiN waveguides.

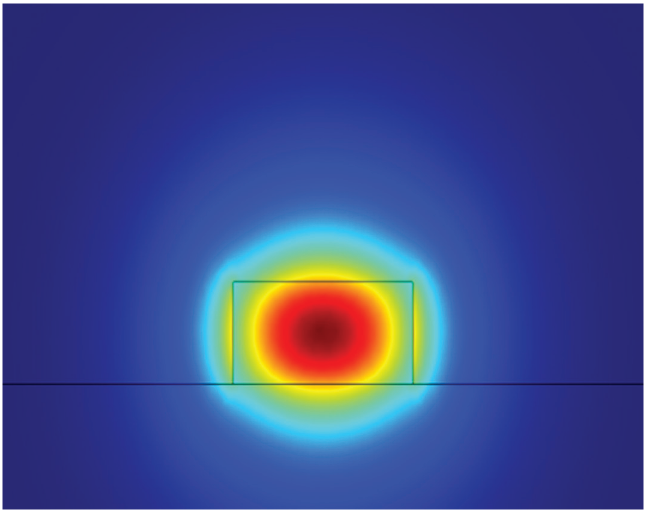

FIGURE 13.10 Mode profile of Si_3N_4 waveguide.

13.3.1 IMPACT OF WAVEGUIDE GEOMETRY ON MODE PROFILES

The geometry of a waveguide plays a critical role in determining its mode profiles, directly influencing the performance and efficiency of integrated photonic devices. Key geometric parameters, such as waveguide width, height, and sidewall angles, govern the spatial confinement and propagation characteristics of optical modes. For SiN waveguides, which are widely used due to their low propagation loss and broad transparency range, the design of these geometric dimensions significantly affects the optical confinement, mode field distribution, and effective refractive index. Variations in waveguide geometry can also impact modal dispersion, polarization dependence, and coupling efficiency with external optical components, such as fibers or quantum emitters. Additionally, advanced waveguide geometries, such as ribbed or trapezoidal designs, may further enhance mode confinement and mitigate fabrication-induced imperfections, such as surface roughness or sidewall tapering. Understanding the interplay between waveguide geometry and mode profiles is therefore essential for optimizing photonic circuit designs, enabling precise control of light propagation for applications in optical communication, quantum technologies, and sensing. This study systematically explores these relationships through numerical simulations and theoretical analysis, offering insights to guide the development of next-generation photonic integrated circuits. Figure 13.11 represents TE and TM mode profile.

The study addresses an essential topic in integrated photonics, particularly the influence of waveguide geometry on mode profiles, which has implications for optical communication and quantum technologies. The use of SiN as the waveguide material is timely, given its low-loss properties and broad applicability in the visible and near-infrared spectrum. The paper presents a well-structured methodology for simulating and analyzing the mode profiles, potentially using established tools like FDTD or FEM. The discussion of geometric parameters (e.g., waveguide width, height, sidewall angles) and their impact on mode confinement, propagation losses, and dispersion is a strong point. The findings are highly relevant for optimizing waveguide design in photonic circuits, enabling improved coupling efficiency and device performance.

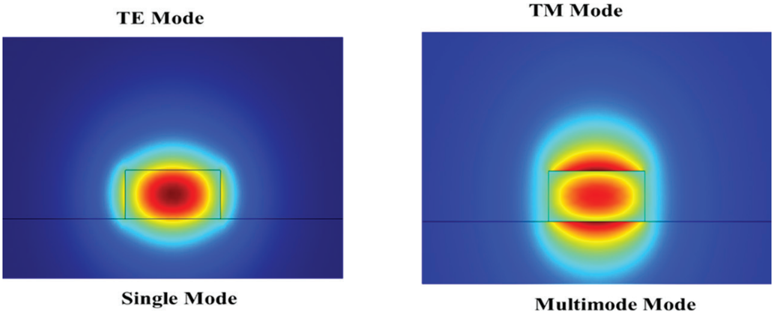

FIGURE 13.11 TE and TM mode profile.

13.3.2 OPTIMIZATION OF SIN WAVEGUIDE DESIGN

The thickness and width of SiN waveguides are pivotal design parameters that significantly influence their optical and functional performance. The thickness of the waveguide primarily controls vertical mode confinement, with thicker waveguides enabling tighter confinement and supporting higher-order modes. However, excessive thickness can lead to multimode operation, which may be undesirable for single-mode applications. In contrast, thinner waveguides promote single-mode behavior but may exhibit higher propagation losses due to weaker confinement and potential substrate leakage. The width of the waveguide dictates lateral mode confinement and affects polarization characteristics, with narrower waveguides improving confinement but increasing sensitivity to sidewall roughness and fabrication imperfections. Wider waveguides, on the other hand, support larger mode areas, reducing coupling losses with external components like fibers, but may introduce dispersion effects that need to be carefully managed.

The interplay between these dimensions also impacts group velocity dispersion, propagation losses, and overall device efficiency. Optimizing waveguide thickness and width is therefore essential for achieving the desired balance between confinement, loss, and compatibility with fabrication tolerances, particularly in SiN-based photonic integrated circuits designed for high-performance optical communication, quantum photonics, and sensing applications. Figures 13.12 and 13.13 depicts mode profile at different heights.

Designing waveguide structures that achieve both low loss and high optical confinement involves navigating critical trade-offs in material properties, geometry, and fabrication processes. High-confinement structures, often required for compact photonic devices, rely on small waveguide dimensions and strong refractive index contrast. However, these features can exacerbate scattering losses due to sidewall roughness and increase sensitivity to fabrication imperfections.

Figure 13.14 represents mode profile at 600 nm width. Low-loss waveguides typically employ smoother interfaces and larger dimensions to reduce scattering and mode leakage, which may compromise confinement and device density. Material

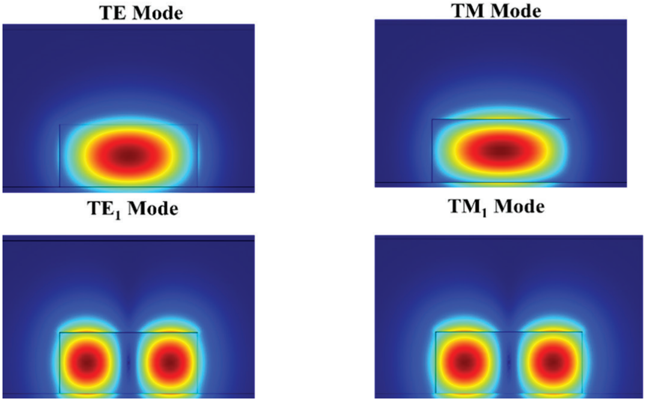

FIGURE 13.12 Mode profile at 400 nm height.

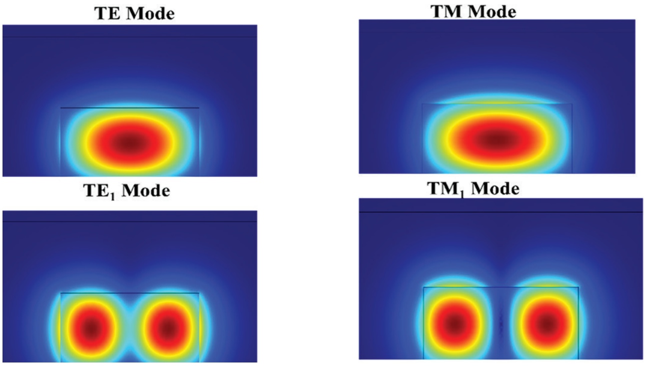

FIGURE 13.13 Mode profile at 500 nm height.

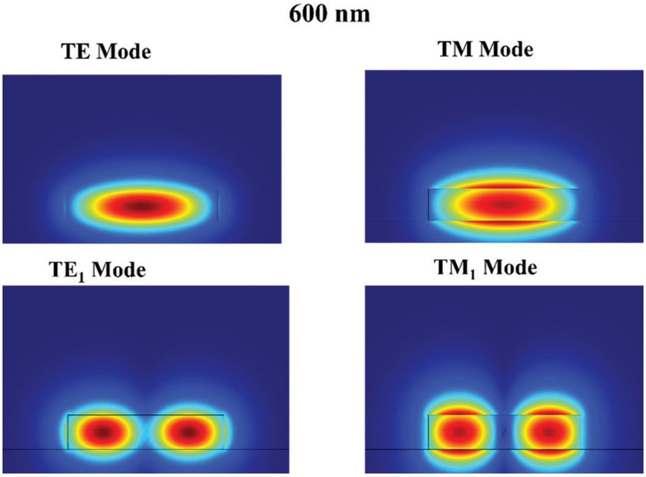

FIGURE 13.14 Mode profile at 600 nm width.

considerations, such as using SiN for its low-loss characteristics and broad transparency range, can mitigate some trade-offs but still require precise control of thickness, width, and etch quality. Additionally, optimizing the mode field overlap with adjacent components, such as fibers or active devices, introduces further constraints. Advanced simulation tools and design optimization techniques are essential for addressing these trade-offs, enabling tailored solutions that balance loss minimization and confinement enhancement for applications in optical communication, quantum photonics, and sensing technologies. Figure 13.15 represents the mode profile at 700 nm width.

Nonlinear photonics plays a pivotal role in advancing quantum computing by enabling the generation, manipulation, and control of quantum states using light. In nonlinear optical materials, the intensity of light can influence its properties, leading to phenomena such as self-phase modulation, four-wave mixing, and second-harmonic generation. These effects are crucial for creating entangled photons,

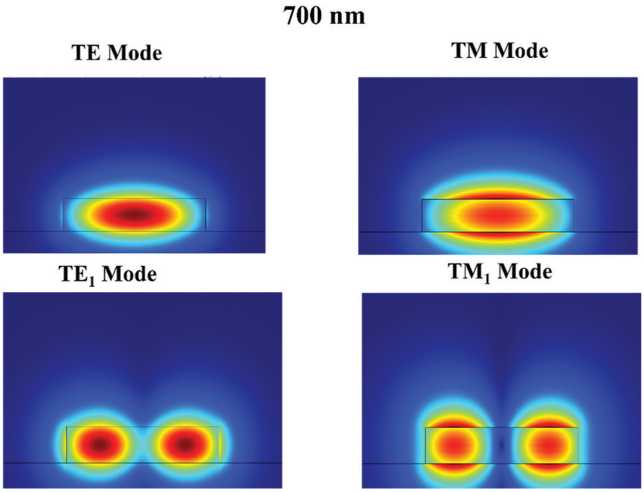

FIGURE 13.15 Mode profile at 700 nm width.

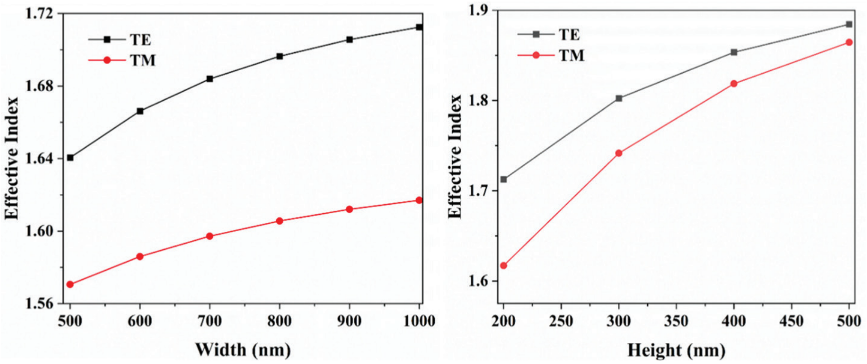

FIGURE 13.16 Variation in effective width with width and height for TE and TM modes.

a fundamental resource for quantum computing and quantum communication protocols. Figure 13.16 represents variation in effective width with width and height for TE and TM modes.

Nonlinear photonic devices, such as waveguides, resonators, and optical cavities, are engineered to exploit these interactions to generate and manipulate quantum states with high fidelity. The integration of nonlinear photonics with quantum computing platforms, including trapped ions, superconducting qubits, and quantum dots, offers new pathways for scalable quantum information processing. Furthermore, nonlinear effects can be used to implement quantum gates, enhance quantum error correction, and facilitate quantum networking, accelerating the development of practical, large-scale quantum computing systems. The synergy between nonlinear optics and quantum technologies holds great promise for revolutionizing fields like cryptography, simulation, and optimization.

13.4 CONCLUSION

The key findings of the study on SiN waveguides highlight several crucial aspects that impact their performance in integrated photonic circuits. First, SiN waveguides offer excellent low-loss characteristics, making them ideal for high-performance optical communication and sensing applications. The study emphasizes the importance of optimizing waveguide geometry, including the width, thickness, and sidewall smoothness, to achieve desired levels of mode confinement and minimize propagation losses. Additionally, it was found that while thinner waveguides improve single-mode behavior and confinement, they may lead to higher losses due to weaker confinement and substrate leakage. Conversely, wider waveguides support larger mode areas, improving coupling efficiency with external components like fibers, but can introduce additional dispersion effects. The trade-off between these parameters is crucial for balancing optical confinement, loss, and device scalability. Finally, future improvements in fabrication techniques and the integration of nonlinear optical effects were identified as key areas for enhancing the performance of SiN waveguides, particularly for applications in quantum photonics and advanced photonic circuits.

In conclusion, SiN waveguides offer significant advantages for integrated photonic circuits, particularly due to their low propagation loss, broad transparency range, and compatibility with advanced fabrication techniques. The ability to finely tune waveguide geometries, such as width, thickness, and material properties, enables the design of highly efficient, low-loss, and compact photonic components. These waveguides are poised to play a crucial role in a variety of applications, from optical communication to quantum computing and biosensing. However, challenges remain in optimizing the balance between confinement, loss, and scalability, especially in high-density photonic integration. Future improvements could focus on addressing fabrication imperfections, such as sidewall roughness, and developing more efficient coupling methods with external components like fibers and quantum devices. Additionally, the integration of advanced nonlinear optical effects could further enhance the functionality of SiN waveguides, enabling new capabilities for quantum information processing and complex optical signal manipulation. As the field progresses, innovations in design methodologies, material science, and fabrication techniques will be essential for unlocking the full potential of SiN waveguides in next-generation integrated photonic circuits.

13.5 MULTIPLE CHOICE QUESTIONS (MCQs)

1. What is the primary advantage of using SiN waveguides in integrated photonic circuits?
   a. High refractive index
   b. Low propagation loss and broad transparency range
   c. High fabrication cost
   d. Large mode area

   Answer: b) Low propagation loss and broad transparency range

2. Which of the following waveguide dimensions has the most significant impact on vertical mode confinement in SiN waveguides?
   a. Width
   b. Height (thickness)
   c. Sidewall angle
   d. Length

   Answer: b) Height (thickness)

3. In a SiN waveguide, increasing the width generally leads to:
   a. Decreased mode confinement and higher scattering losses
   b. Increased mode confinement and reduced scattering losses
   c. Decreased coupling efficiency with external components
   d. Increased group velocity dispersion

   Answer: a) Decreased mode confinement and higher scattering losses

4. What is a common challenge associated with narrow SiN waveguides?
   a. Increased propagation loss due to scattering
   b. Difficulty in achieving single-mode operation
   c. Low coupling efficiency with external components
   d. Increased refractive index contrast

   Answer: a) Increased propagation loss due to scattering

5. Which of the following factors significantly affects the fabrication quality of SiN waveguides?
   a. Waveguide width
   b. Sidewall roughness
   c. Material refractive index
   d. Temperature stability

   Answer: b) Sidewall roughness

6. What is a typical application of SiN waveguides in photonic integrated circuits?
   a. Quantum computing and optical communication
   b. Light-emitting diode (LED) fabrication
   c. Semiconductor manufacturing
   d. Solar cell energy conversion

   Answer: a) Quantum computing and optical communication

7. Increasing the thickness of a SiN waveguide typically results in:
   a. Reduced mode confinement
   b. Increased single-mode behavior
   c. Increased propagation losses due to weaker confinement

   d. Support for higher-order modes

   Answer: d) Support for higher-order modes

8. Which property of SiN waveguides can be enhanced by optimizing waveguide dimensions?
   a. Mode profile and dispersion characteristics
   b. Heat resistance
   c. Optical gain
   d. Electric field strength

   Answer: a) Mode profile and dispersion characteristics

9. The primary reason for using SiN over silicon in waveguide applications is:
   a. Higher refractive index
   b. Lower fabrication cost
   c. Better performance at high temperatures
   d. Lower propagation loss and broader transparency range

   Answer: d) Lower propagation loss and broader transparency range

10. For achieving high coupling efficiency between SiN waveguides and optical fibers, which factor is most critical?
    a. Waveguide length
    b. Mode profile and mode matching
    c. Refractive index of the substrate
    d. Temperature stability

    Answer: b) Mode profile and mode matching

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